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Performance study of a HEMT for power application

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Abstract

In this paper, we present a simulation results of the design and characterization for GaN double-gate transistor, that has T-gate geometries with high-electron-mobility to realize high performance using silvaco TCAD Software, this transistor is used for amplifiers application. We have obtained an excellent current density, almost 817mA/mm, a peak extrinsic transconductance of 915mS/mm at V_{DS}=2 V, and cutting frequency cutoffs of 878 GHz, and maximum frequency of 982 GHz.

Keywords— HEMT, GaN, power application, Tcad-Silvaco.

I. Introduction

Currently, Devices that work as a low-noise amplifier when the input signal level is low and automatically switches to high-power amplification for relatively high input signal levels [1] are the future of amplification.
For that we can enhance the performances of the next-generation with GaN-based high electron mobility transistors, we have created the structure using genetic algorithm and using Silvaco software tools for simulation.

The introduction of a thin AlN spacer layer at the InAlN/GaN interface, increases the carrier density and effectively reduces the alloy scattering of the two-dimensional electron gas (2DEG), so that it provides a better carrier confinement [2-3], InAlN/GaN heterostructure has good thermal stability and robustness, promising very high power and high temperature work operating mode [4].

A hydrodynamic or quantum model approach must be used to obtain accurate results for such structures. We propose quantum mobility models which corresponds to the particularities of the GaN material system. The models was implemented in our simulator Silvaco and carefully calibrated. A device from a recent transistor generation is simulated using the quantum genetic. A good accuracy for all relevant characteristics is achieved.
In this work, we have demonstrated that is possible to produce excellent properties of HEMT InAlN / GaN while minimizing side effects. Through the optimization of the device design and quality control of doping implant, also the adoption of several analytical models to simulate the devices highly scaled analysis characteristics [5], [6], in order to intentionally decrease phenomena unwanted until they become almost negligible.

2. Modeling Results

As illustrated in fig.1 (a), we see a cross section of the structure, and this structure located over the layer of substrate (4H-SiC). The device contact used an Au Schottky source/drain and gate electrodes, the device design features a heterostructure InAlN/GaN, where the periphery oxide Al_2O_3 of the Gate is a different than the conventional designs [7], and the passivation dielectric that minimizes surface leakage and creates a high density of shallow traps at the surface [8]. As a result, after a doping layer the leakage current density is eliminated from the device, resulting in an InAlN barrier undoped [9].

This raises the conduction band shape for the barrier that, for the same sheet carrier concentration based on Fujitsu model [10], The Hall mobility and sheet carrier concentration were 1300 $cm^2 V^{-1} s^{-1}$ and 1×10^{13} cm^{-2}.The heterojunction features a sheet charge density of $1.85x\ 10^{13}$ cm^2.Dimensions are also critical parameters for the device performance, the dimension of the device studied is given in Table 1.

Table 1 : Parameters of HEMT device.

Name	Symbol	Value [nm]
Thickness Cap Layer	E_{OH}	3
Thickness Layer Schottky	E_S	7
Thickness Layer Donor	E_D	3
Thickness Layer Spacer	E_E	1
Thickness Canal Layer	E_C	37
Thickness Tampon Layer	E_T	150
Thickness of Bulk	E_B	$100\ 10^3$
Length Drain Gate1	L_{DG}	$1.47\ 10^3$
Length Source Gate2	L_{SG}	$0.50\ 10^3$
Length Gate	L_G	15
Length Drain & Source	L_D	$0.5\ 10^3$

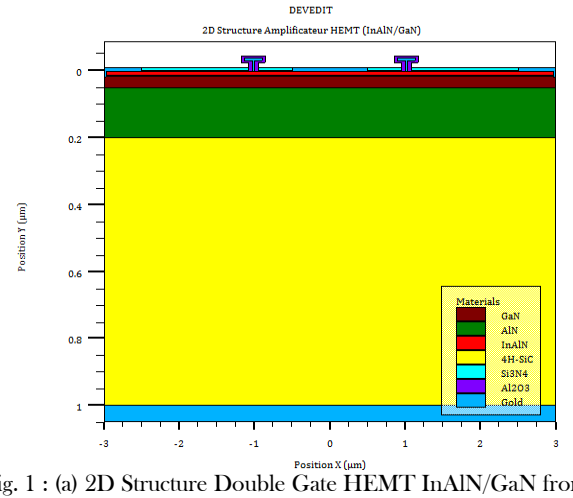

Fig. 1 : (a) 2D Structure Double Gate HEMT InAlN/GaN from Atlas.

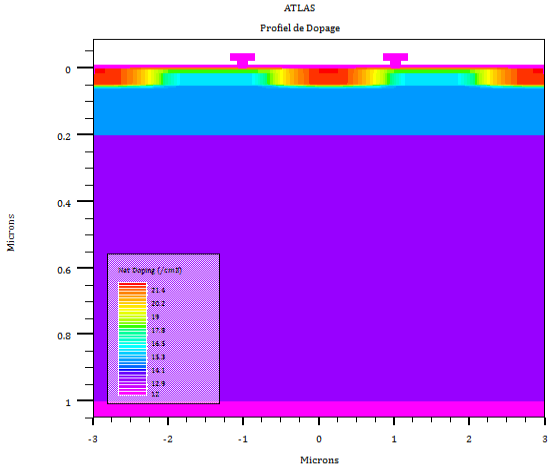

Fig. 2 : (b) Doping profile.

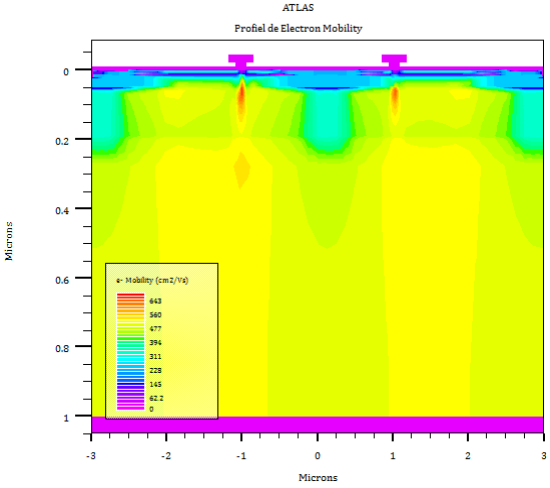

Fig. 3 : (c) Electron mobility.

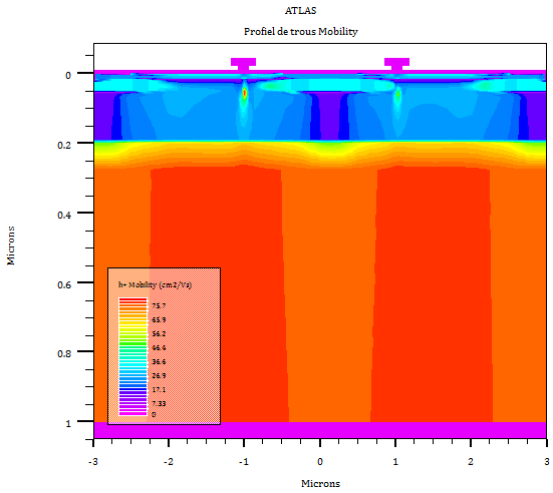

Fig. 4 : (d) Holes mobility.

3. Results and discussion

In this work, Silvaco ATLAS is used for the 2D simulation of the considered HEMT. Silvaco's ATLAS program performed the device structuring and subprogram calls, while BLAZE and GIGA, ATLAS sub-modules, perform special functions required for advanced materials, hetero-junctions, and thermal modeling. In fact, ATLAS generally uses the BLAZE program extension to correct model for the III-V semiconductors, in order to adapt calculations that involve energy bands at the hetero-structure. The hetero-junctions need to change in determination of current densities, recombination-generation and velocity saturation. The hydrodynamic with energy balance carrier transport model is used in order to achieve maximum accuracy as computational efficiency.

However, while using TCAD simulation software, some of physical models have to be incorporated into the model to perform desired simulations and do reliable predictions about our device characteristics.

These models deal with the carrier behavior such as lattice temperature. In addition, because of the high operating voltages, self-heating effects need to be considered in our simulations.

A. DC Results

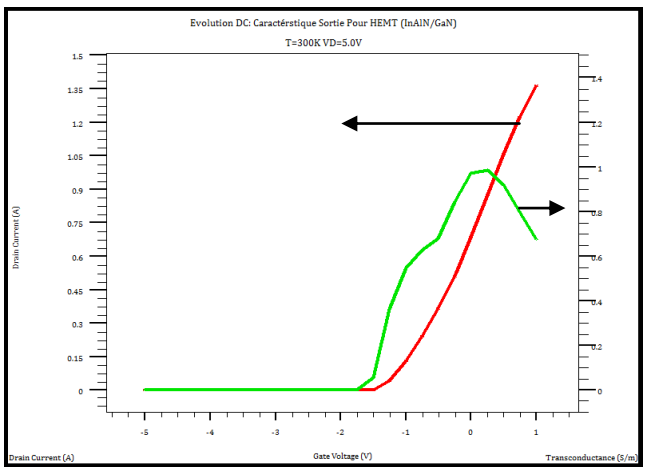

Fig. 5 : characteristics of HEMT InAlN/GaN with a gate length of 15 nm with V_{DS} 2.0 V.

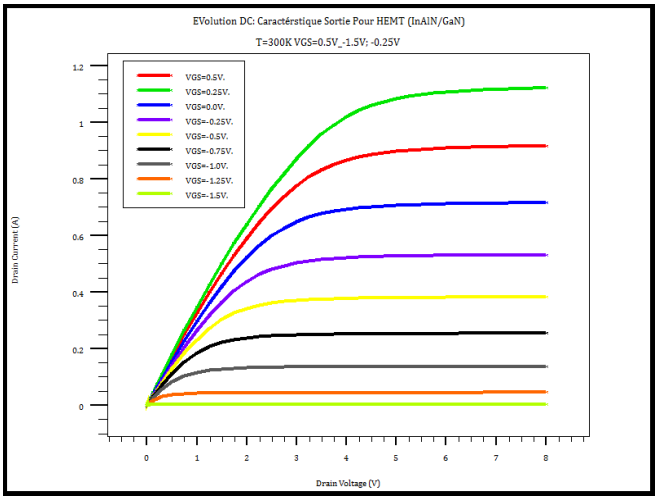

Fig. 6 : DC Output characteristics of DG-HEMT InAlN/GaN with a gate length of 15 nm with V_{GS} stepped from 0.25 V to −1.5 V in steps of −0.25 V.

In this simulation of the devices the electrical characteristics transfer is illustrated in right of the Fig. (2) The HEMTs with a gate length of the 15 nm, the device is delivered to extract an ON/OFF current density ratio higher than 1 x 10^{10}, and we have investigated the conduction band profiles to show that drain-induced barrier lowering (DIBL) is more explicit in a highly scaled device at length gate 15 nm,DIBL=33.52mV/V with V_{DS} fixed between 2 V and V_{DD}, effects due to this length of the gate which are observed are called short-channel effects (SCE). Effects occurring at larger V_{DS} are termed drain induced barrier lowering (DIBL) effects [11]. We are not the first to observe this in simulations for HEMTs, it has been investigated since 1989 by Awano and al. [12].

Fig. (2) in left we have presented the extrinsic transconductance characteristics of the device at V_{DS}=2 V, the simulated exhibits a maximum as 915mS/nm at V_{GS}=0.0 V. This peak shows in the curve of the transconductance a dependence on gate bias V_{GS} and obviously reflects the DC behavior of the simulated HEMT, which correspond to the 2DEG channels modulated by different gate voltages. These properties are superior to the values previously reported for similar structures based on AlGaN/GaN heterostructures [13]. Here, a better DC characteristic is realized on sample with slight inferior electrical properties in comparison with the earlier reported [14], the total parasitic resistance generally is dominated at low Ohmic contact resistance for this is to highly desirable, which could be attributed to the increased carrier concentration or/and an increased carrier mobility [15].

We have changed the drain voltage between 0V and 3V, when simulation is first conducted to obtain the I-V characteristic in DC mode to change the state of the gate voltage by 10 different bias, V_{GS} = 0.25 V to - 1.5V with the step of the -0.25V for both HEMTs. The positive increase in the drain voltage, leads to the electric field across the channel increases the speed of the electron. The voltage distribution across the channel leads to a voltage difference between the gate and the channel along it, the transistor taking a variable resistance behavior controlled by the gate voltage. Indicating excellent gate control of the 2DEG channel [16], and the maximum drain current available reached 817 mA/mm when V_{GS} was biased at 0.0 V & V_{DS}=3.0V. The pinchoff voltage is extracted at −1.5 V. show in Fig. 3.

B. AC Results

We Show in this simulation the gain of the current H_{21}, unilateral (U_T), max transducer (MGT), maximum stable (GMS) and maximum available (GMA) for power gain versus frequency range of [1 GHz to 1 THz] in fig 5.

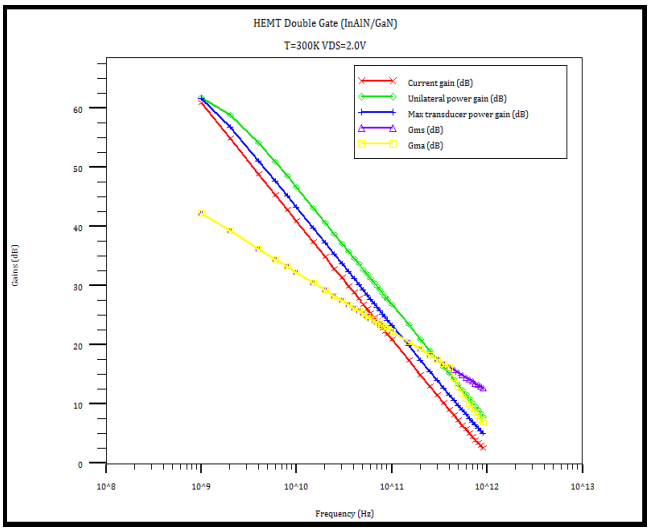

Fig. 7 : Simulated current gain (H_{21}), Unilateral (UT), max transducer (MTG), max available (GMA) and Max stable power gain (GMS) versus frequency for the L_G=15nm InAlN/GaNHEMTs. The bias were V_{DS}=5VandV$_{GS}$=0V.

This result values extracted after verifying from the extrinsic S-parameters with the intrinsic values of this device by simulation with extrinsic parameter models, due to the effect of the capacitances of the high gate to source capacitance (C_{GS}) resulting from the extended effective gate length [18], and the electronic transfer in the channel is optimized.

The cutoff frequency is 978 GHz and the value of Max frequency is approximately of 889 GHz with a slope of 0 dB/Dec for the device, this value is greater than DG-HEMT and may be used for future low noise MMIC design applications.

Inset shows that the peak value of GMS and GMA is obtained as 42 dB and for U_T, GMT and H_{21} are 61 dB, 62 dB and 63 dB through simulation respectively. A steep decrease is observed up to around 0 dB for frequencies even it is greater than 1 THz. This indicates good stability performance exhibited by the device making it suitable for low-noise amplifier applications.

The rise in the value of the frequency of the pieces show the basis for being associated with the length of the gate, gas electron two-dimensional gas is double 2DEG in the canal, as well as the design of the device. For comparison, the highest ft reported so far in nitride transistors double gate was the device is enhanced and very impressive f_T and f_{Max} peak values of 668 GHz and 312 GHz are obtained respectively [19].

4. Conclusion

In this paper, we have reported high-efficiency GaN HEMT on SiC substrates using the periphery Al2O3 oxide periphery of the gate and the mince InAlN barrier for

amplifier applications. Balanced device was designed and simulated by using a GaN HEMT by Tcad-Silvaco software.

The results prove that the proposed GaN HEMT amplifier can deliver the highest power and higher efficiency performances for power applications.

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Implementation of a maximum power point tracking (MPPT) Algorithm for photovoltaic (PV) system

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Abstract:
Solar energy is a clean and promising source of energy that can be adapted perfectly with multiple systems. The electrical characteristic of the Photovoltaic generator contains an optimal operating point generally called the maximum power point. For this, the implementation of a tracker of the maximum power point is necessary. They play a critical role in photovoltaic (PV) power system for maximize the power of the GPV under different irradiance conditions. This paper deals a strategy for optimizing the performance of a photovoltaic system under real climatic conditions. The maximum power point tracking "MPPT" used in this paper is the perturbation and observation (P&O) algorithm. A controlled Boost DC–DC converter was implemented and connected to a SunTech STP085B PV panel to verify the accuracy of the proposed method. Matlab/Simulink was used for the simulation studies. A digital signal processor (dSPACE ACE1104) based controller was constructed to implement the proposed MPPT control, and the experimental results are presented.

Keywords: Solar energy; Maximum Power Point Tracking; perturbation and observation algorithm;dSPACE controllerBoost converter

1. Introduction

The renewable energy plays a very important role in the production of electricity, mainly in developed countries. The sun is a clean, renewable and not polluting source to generate electricity. The electricity production in systems based on solar cells, where the solar photons are absorbed by a semiconductor is directly converted into electrical energy [1].

The characteristic of the photovoltaic generator (PVG) depends on the temperature, and the irradiation solar. The electrical characteristic voltage/power of the photovoltaic generator (PVG) represents the variation of the power according to the voltage across the photovoltaic generator. In this characteristic, the photovoltaic generator contains an optimal operating point generally called the maximum power point, located in a non-linear zone. To improve the efficiency of the photovoltaic system, the implementation of a tracker of the maximum power point (MPP) is necessary.

There are several methods to obtain the maximum power of the photovoltaic generator [2- 4] can be divided into two groups; offline methods and online methods[5]. These methods differ in terms of complexity, speed of response, amount of investment, the number and types of sensors required and the hardware implementation [5]. Offline methods commonly used the short circuit current and open circuit voltage of the GVP. Generally there are two well-known methods are; the open circuit method [6], and the short circuit current method [7], the authors [8] have been proposed the new offline method based in Artificial Neural Networks (ANN).

In online methods, the current and voltage of the solar panel are measured instantaneous; the most famous in this group are: Perturbation and Observation (P & O) [9], incremental conductance [2], the Ripple Correlation Control (RCC) [10], hill climbing, the three point's comparison and the feedback methods of power [11].

There are author used the methods based on «artificial intelligence» such as the authors [12 - 14] have proposed the maximum power point tracking (MPPT) algorithm based on artificial neural networks. The author [13] proposed genetic algorithms, and the author [15 - 17] have used fuzzy logic to obtain the optimum power point

In this paper, optimizing the performance of a photovoltaic system with Perturbation and Observation (P & O) algorithm, In Section 2 The solar panel modeland a Boost converter model are presented. Section 3 the photovoltaic system for tracking maximum power is introduced. Section 4 our method for tracking the maximum power is presented "the P and O algorithm" section 5 the experimental setup and results are presented to demonstrate the efficiency of the proposed system. Finally the conclusion are presented

2. Photovoltaic generator

There are several models mathematics used for simulate the photovoltaic generator. These models differ in the method of calculation and the number of parameters involved in the current - voltage characteristic.

In our case, we chose a simple model that requires the parameters given by the manufacturer.

We have implemented the five parameter model. The equation for the model of the photovoltaic cell involves the relationship between the output voltage and the current. To increase the output power of the system, solar cells are generally connected in series and/ or in parallel to form PV modules.

This model can be summarized as follows: [18 -20]

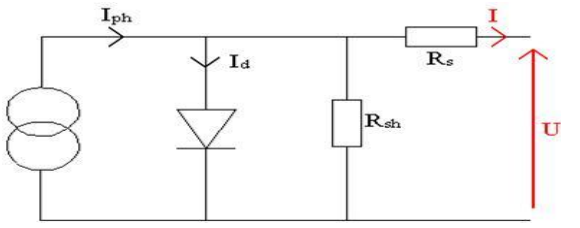

Figure 1. The solar cell

The output current of the solar cell is given by

$I = I_{ph} - I_d - I_{sh}$

By considering the electrical characteristics of a junction, this current can be given by

$$I = I_{ph} - I_0\left(e^{\frac{q(U+IR_S)}{AKT}} - 1\right) - \frac{U+IR_S}{R_{sh}} \qquad (1)$$

When one replaces the term VT = KT/q, one finds

$$I = I_{ph} - I_0\left(e^{\frac{(U+IR_S)}{AV_T}} - 1\right) \qquad (2)$$

The third term in equ (1) is neglected because R_{sh} is bigger than R_s

The output voltage of the cell becomes

$$U = -IR_s + \frac{AKT}{q}\ln\left(\frac{I_{ph} - I + I_0}{I_0}\right) \qquad (3)$$

Where:

R.: series resistance

R_{sh}: shunt resistance

I_{ph}: short circuit current

I_d: current of the diode

I_{Rsh}: current of the parallel resistor Rp

I: output current and of the solar cell

U: output voltage of the solar cell

I_o: reverse saturation current of the diode

q: charge of the electron

A: diode ideality factor

K: Boltzmann constant

T: temperature in °K

For the rest of our work, we have chosen a STP085B PV module. It consists of 54 polycrystalline silicon solar cells connected in series and provides a nominal power 85W. The electrical parameters are given in Table 1.

Table 1. Module STP085B

$I_{short-Circuit}$	$V_{Open-Circuit}$	$V_{Maximum}$	$I_{Maximum}$	$P_{Maximum}$
5.15 A	21.9V	17.8V	4.83 A	85W

The photovoltaic generator (PVG) is composed by cells solar connected serially and/or parallel. Voltage and current of PVG is proportional to the number of series and parallel cells respectively.

From the last equation, the characteristics of the solar module I = f (V), with a variable illumination, will have the following form (for a junction temperature of 25 ° C and a spectral distribution of said radiation of AM 1.5).

Note that the voltage Voc varies very little according to the illumination, unlike the current I_{sc} increases strongly with the illumination.

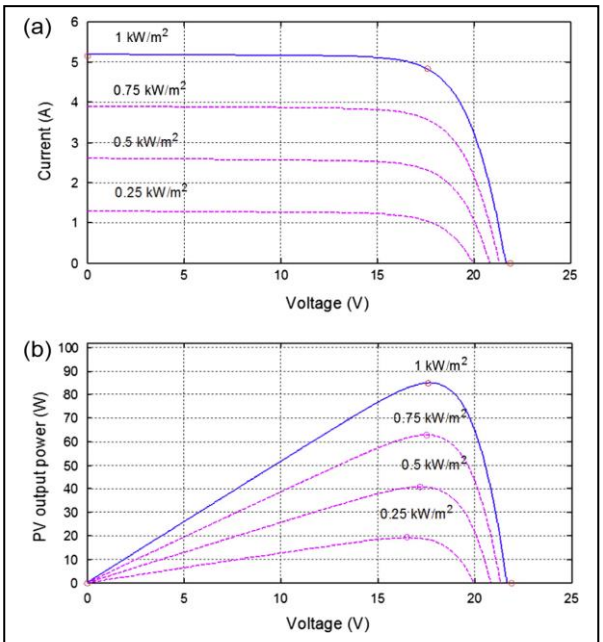

Figure 2. (a) I–V characteristics and (b) P–V characteristics with varying irradiation.

3. DC-DC Converter

The boost converter is a type DC-DC converter composed principally by Electronics components. It is used in several domains. In this case, the boost converter coupled with PVG. Maximum power point tracking "MPPT" controller generated the duty cycle will be controlled the MOSFET of Boost converter to maintain the power of PVG it near from the maximum power point, whatever of the variations of the

illumination. The following figure shows circuit the boost converter: [20]

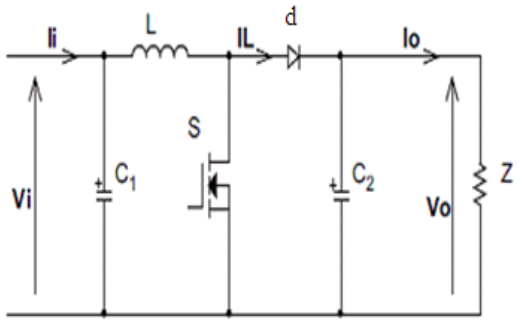

Figure 3. The Boost converter.

The mathematical model of the DC-DC converter expressed by the following equations: [20, 21]

$$\frac{V_0}{V_i} = \frac{1}{1-D} \quad (4)$$

$$\frac{I_i}{I_0} = \frac{1}{1-D} \quad (5)$$

$$I_L = I_i - C_1 \frac{DV_i}{dt} \quad (6)$$

$$I_0 = (1-D)I_L - C_2 \frac{DV_0}{dt} \quad (7)$$

$$V_i = (1-D)V_0 + R_L I_L L \frac{DI_L}{dt} \quad (8)$$

Where:

I: input current
Io: output current
V_i : input voltage
V_o: output voltage
d: diode
D:duty cycle
L: inductance
S: switch
C_1, C_2: capacitances
Z: output impedance

The critical values of the inductance and capacitance can be calculated using the following equations:

$$L = \frac{(1-D)^2.D.R}{2.f} \quad (9)$$

$$C = \frac{D}{2.f.R} \quad (10)$$

4. Maximum power point tracking

Maximum power point tracking "MPPT" controller play a critical role in photovoltaic (PV) power system for maximizes the power of the PVG. The role of maximum power point tracking "MPPT" controller is to search the maximum power point of the PV system. The control principle is based on the automatic variation of the duty cycle D to the appropriate value so as to maximize the power output of the PV panel. There are different type's algorithms of the MPPT controller [22].

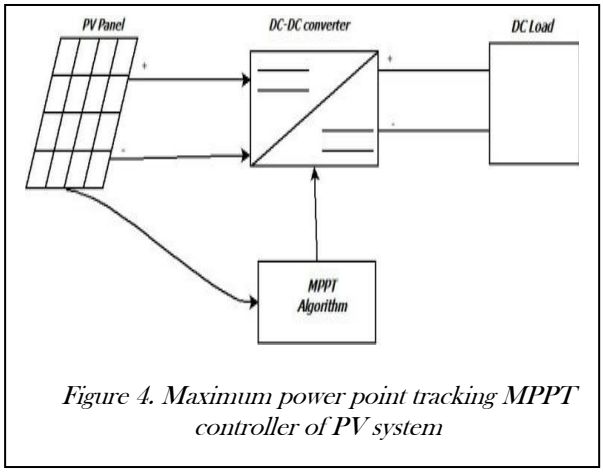

Figure 4. Maximum power point tracking MPPT controller of PV system

5. The P & O algorithm

The P & O algorithm is the most commonly exploited to search the point of maximum power, due to its simplicity and requires only voltage and current measurements of the PVG.

Operating principle based on perturbation of voltage and observing the impact of this change on the output power of the PV panel. At each cycle, and I_{pv}, $V_{pv}$are measured to calculate P_{pv} (k). The value P_{pv} (k) is compared with the value P_{pv} (k -1) calculated in the previous cycle.

If the output power has increased, Vpvis adjusted in the same direction as in the previous cycle. If the power output has decreased, Vpvis adjusted in the opposite direction as the previous cycle direction. It uses an iterative method. The table 2 bellow summarized the operation of the P&O-MPPT algorithm

Table 2
The principle operation of the P&O-MPPT algorithm

Case	ΔP	ΔV	Action
4	P(k) > P(k-1)	V(k) > V(k-1)	V++
3	P(k) > P(k-1)	V(k) < V(k-1)	V--
2	P(k) < P(k-1)	V(k) > V(k-1)	V--
1	P(k) < P(k-1)	V(k) < V(k-1)	V++

A scheme of the algorithm is shown in Figure 5.

If the step size is very small losses in states stable or slowly changing conditions will reduced, but the system has a slow response to rapid changes in temperature or exposure.

The ideal value for the width of the system cannot be determined experimentally or by simulation, thus meet a compromise between rapid response and loss power in stable state.

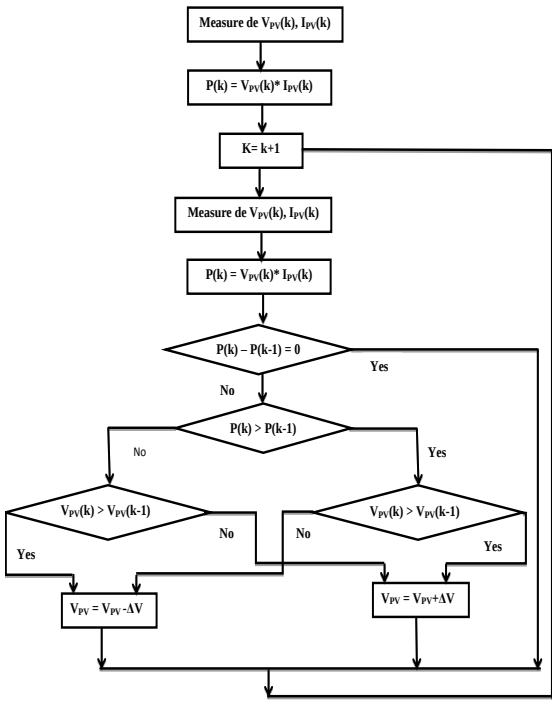

Figure 5 Organization of the disturbance and Observation (P and O) algorithm.

6. Experimental Setup

The proposed MPPT algorithm is implemented using a digital controller based on a dSPACE DSP unit. The DS1104 R&D Controller Board upgrades your PC to a development system for rapid control prototyping (RCP). The real-time hardware – based on the PowerPC 603e microprocessor – and its I/O interfaces make the board ideally suited for developing controllers in various fields – in both industry and university.

The dSPACE is a powerful tool to modify the MPPT controller parameters real time and to monitor real processes while an experiment is operated. The system components are:

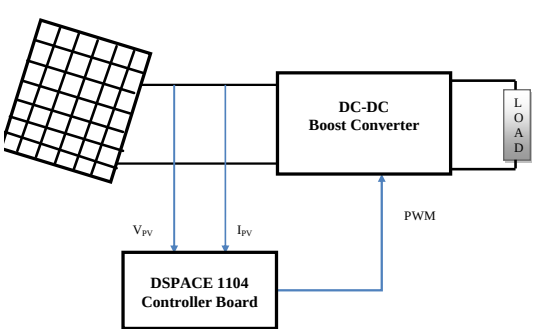

Figure 6.Configuration of a PV power Control system

The bench test was based on the following equipment: four real Suntech85 W panels (used in the LAS laboratory in Sétif, Algeria), a Semikron DC-DC Boost converter operating with a switching frequency of 10 kHz and a variable resistor as a load. A Hall Effect CT LEM (PR30) and a HAMEG HZ64 isolation amplifier were used to detect the PV output current and PV output voltage.

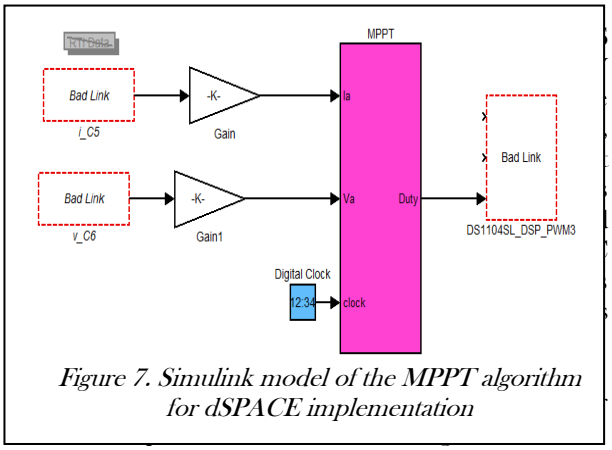

Figure 7. Simulink model of the MPPT algorithm for dSPACE implementation

7. Experimental Results

To test and verify the performance of the MPPT controller with perturbed and observe algorithm were performed on experimental prototypes designed and built in LAS laboratory in Setif "Algeria". A system of four PV solar panels was used as the resistance from 33 Ohm.

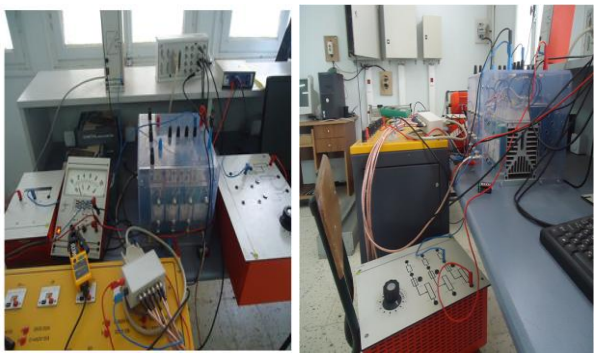

Figure 8. The bench test

The experimental results of the proposed system were implemented using DSPACE DS1104 is presented in figure 9, 10, 11and 12.

The experimental duty cycle is shown in Fig. 9. The experimental PV output voltage and current are shown in Fig. 11 and 10, respectively. The electrical

characteristic of the photovoltaic generator (PVG), I = f(V) and P = f (V) are represents in Fig. 12.a and 12.b, respectively.

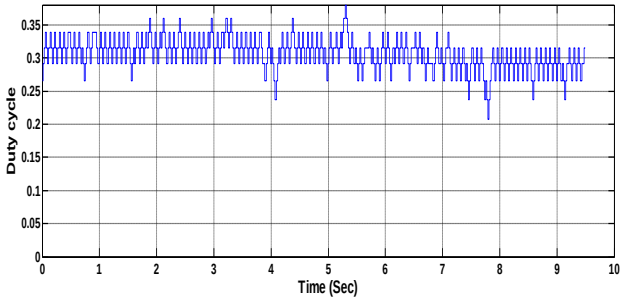

Figure 9. Duty cycle

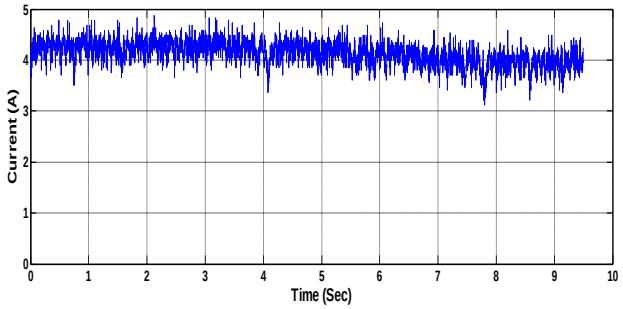

Figure 10. Experimental maximum PV current

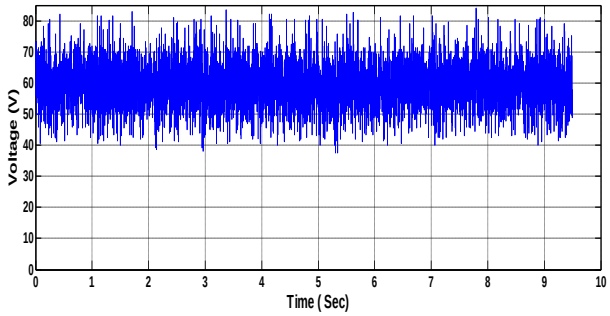

Figure11. Experimental maximum PV voltage

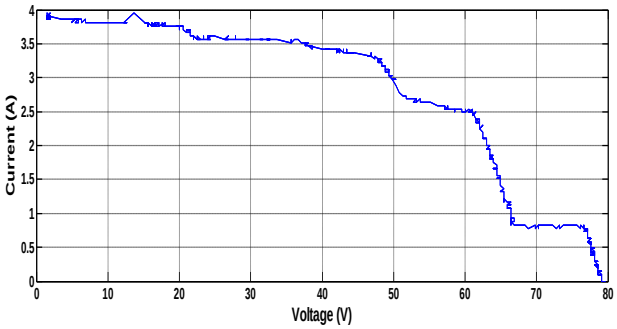

Figure 12 (a) Experimental I-V curve of a photovoltaic panel

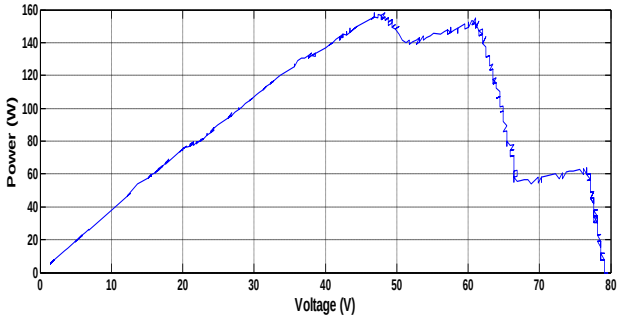

Figure 12 (b) Experimental P-V curve of a photovoltaic panel

8. Conclusion

The principal objective of this study is to improve the performances of a photovoltaic system under real climatic conditions. For this, we have used the MPPT control based on perturb and observe algorithm connected in boost converter. The system demonstrates acceptable response under real climatic conditions. A dSPACE ACE1104 based controller was used to implement the proposed MPPT and control algorithm. The experimental results are presented to verify the performance.

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Temperature variation effects in partially depleted SOI n-channel MOSFETs

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Abstract:
Silicon-on insulator (SOI) technology has attracted a great attention as a probable alternative candidate for low power, high performances applications. Nowadays electronic is subjected to temperature variations and is, some time, obliged to operate at high temperature. In this paper, based on some simulations results we obtained using ATLAS SILVACO TCAD software, we have investigate the impact of temperature variation on the electrical properties of a PD SOI n-MOSFET. This study allows us to highlight the existence of a ZTC point as well in the linear that in the saturated region. We also examine the off state leakage current dependence with temperature. At the end of this workself heating effects are also studied.
Keywords: Temperature effects; SOI MOSFETS, ZTC point, self heating effects, leackage current.

1. Introduction

Electronic is continually and always subjected to temperature variations, and is consequently constraint to operate at different temperatures. The typical examples are that of the automobile, the military, the space, and the nuclear industries. In these industries integrated circuits "ICs" used are often constrained to operate at very high temperatures much beyond 150 ° C. Knowing that semiconductors are very sensitive to temperature variations,it becomes crucial to understand the phenomena caused by these variations and their implications. These implications do not occur only on physical quantities but also on the electrical ones of designed devices conceived for applications where temperature variation or high temperature applications are expected. The operating temperature of components and consequently of circuits has a direct influence on their electric characteristics. A high operating temperature leads undeniably to their ageing. Temperature variations deteriorate ineluctably the correct operation of analog and digital ICs in terms of power dissipated in stand-by mode, speed, and accuracy. As a result, various technologies have been investigated as being a probable alternative intended for operations particularly at high temperatures. These explored technologies comprise GaAs [1], CMOS [2] and SOI [3] technologies. At high temperature, CMOS technology is unfortunately restricted in its operation by the existence of latch up phenomenon inherent in this technology, and by the presence of high leakage current through its well junction. Hence, other materials, such as III-V, SiC or diamond, have the ability to operate above 500 ° Celsius, but have unfortunately not the necessary maturity to be exploited to short or even medium term. While GaAs seems much more favorable than silicon for high temperatures application, it remains largely supplanted by SOI-CMOS technology in terms of stability with respect to temperature fluctuations. Indeed, the use of SOI- CMOS devices seems to be an excellent alternative to operate at high temperature, this is of course essentially due to the absence of latch-up phenomena with a sufficient reduction of leakage current

In this paper, we will investigate the temperature variation effect on the I_{DS}–V_{GS}, I_{DS}–V_{DS} and gm–V_{GS} characteristics , we will also investigate the zero temperature coefficients biasing point called "ZTC" of SOI MOSFETs using ATLAS SILVACO software. We will also examine the impact of temperature variation effect on the off state current of our device. At the term of this workself heating effects are also presented.

2. Overview of SOI technology

In the 1960's the necessity for radiation hard devices in the military and space industry had lead to the development of silicon on-insulator devices. During 1970s and '80s some SOI materials and structures were designed for dielectrically separating the thin active device volume from the silicon substrate.

SOI technology has several industrial processes that have been developed in order to make a Silicon film on an insulating layer called buried oxide "BOX". The oldest process is the Silicon-On-Sapphire called "SOS" and also called hetero-epitaxy process, in view of the fact that silicon and sapphire are different materials with different crystallographic structures. SOS substrates are obtained by growing a thin silicon film on the top of a monocristalline sapphire substrate. Since the 1980s, other techniques have been developed and have become industry standards. The two main processes are Separation by Implantation of

Oxygen called SIMOX and Bounded SOI Wafer called BSOI [4], [5]. In SIMOX process, considered as the dominant technology this last decade, oxygen ions are implanted below the surface of a bulk Si wafer, after that, a thermal annealing allows creating a SiO2 layer buried inside this wafer. In BSOI process, wafer bonding materials can be obtained by gluing two wafers togetherand creating hydrogen bonds between these two wafers.Primary, a bulk silicon wafer (wafer A) is oxidized then, a high-energy implant of hydrogen ions is carried out in order to generate defects at a fixed depth in this wafer, by using hydrophilic bonding, it is then bonded to a second silicon bulk wafer (wafer B). After a thermal annealing, the wafer A is divided into two parts, a small monocristalline silicon which remains bonded to the wafer B, and the rest of the wafer A [6],[7]. SIMOX and BSOI are considered as being the main processes [4], [5].; with a technique derived: the Smart Cut technology. This technique currently dominates the SOI market, and represents about 90% of actual SOI production [8].

SOI MOSFETs that are built on a thin silicon layer situated on the top of an insulator layerprovides a robust vertical isolation from the substrate and reduces dramatically the junction capacitance [9],thus doing this device much faster than a standard silicon-based device. If the thin silicon film, used to build active devices and circuits, is thin enough the depletion zone below the gate extends all the way through the BOX, and the device shown in Figure 1.A is called fully depleted, if not, and generally if the silicon film is currently thicker than 100 nm as shown in Figure 1.B it is called partially depleted. The much important characteristic of FD SOI MOSFET is that the current drive is higher than in bulk MOSFET and its subthreshold slope is sharper due to an much smaller body factor [10].

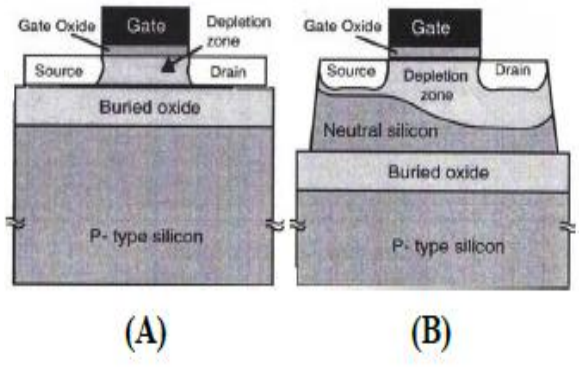

Figure 1. (A) - Fully depleted SOI MOSFET. (B) -Partially depleted SOI MOSFET [11].

Generally, SOI MOSFETs owning a thin SOI layer (usually lower than 50 nm) with all body areas under the channel depleted are called fully depleted SOI MOSFETs (FD-SOI). Conversely, SOI MOSFETs, owning a thick SOI layer (usually greater than 100 nm), with some areas at the bottom of the body area that are not depleted, are called partially depleted SOI MOSFETs (PD-SOI).

3. SOI MOSFETs operation according to depletion zones Thickness

Silicon active layer thickness, t_{si}, is the most important parameter in the classification and operation of SOI MOSFETs. According to this thickness, localized between the BOX and gate oxide, SOI MOSFETs operation and various physical phenomena in these components change [8].

In SOI devices, both of the gate/oxide gate/ body and substrate/ buried oxide/body form a metal-insulator-semiconductor structure. As a result two depletion zones are present in the active region. The first region is controlled by the top gate when the second region is controlled by the substrate that is considered as a back gate. Each gate requires a surface potential for its Si/SiO2 interface and an operating regime: accumulation, desertion, inversion. When the metal-insulator-semiconductor structure operates under strong inversion the depletion zone thickness is maximum and equal to X_{dmax}. In this case, the surface potential is nearly equal to $2\Phi_F$. Under these conditions the maximum depletion width X_{dmax}, for a PD MOSFET of each depletion zone can be expressed by [12]:

$$X_{dmax} = \sqrt{\frac{4.\varepsilon_{si}.\emptyset_F}{q.N_A}} \qquad (1)$$

$$\emptyset_F = \frac{k.T}{q}.\ln\left(\frac{N_A}{n_i}\right) \qquad (2)$$

Where $\varepsilon_{si}$is the relative dielectric permittivity of silicon(F/m) , N_A the Silicon layer doping (cm^{-3}), Φ_F the Fermi potential(V), n_i the intrinsic electron density (cm^3), K Boltzmann's constant (eV/°K), q the Electron charge(cb) and T the temperature (°K).

The depletion conditions according to depletion zone thickness Xdmaxare summarized in table 1.

TABLE I
SOI MOSFET Operation according to depletion zones thickness.

	$T_{si}<X_{DMAX.}$	$X_{dmax}<t_{si}<2_{max}$	$t_{si}>2\ X_{dmax}$
Silicon film	Fully Depleted mode	Not Fully Depleted .Depend on bias conditions.	Partially-Depleted-mode.

According to biasing conditions and doping conditions, the two depletion zones cover partially or totally the silicon film of the active zone.

4. Temperature parameters sensitivity of the PD SOI n-MOSFETs.

The PD SOI n-MOSFETS may be considered because of the neutral region in the fin film, as an association of a MOSFET transistor located in the top portion of thin film and a parasitic BJT located in the bottom portion of this thin film. The device temperature-dependent parameters, mentioned briefly in the following, include electron mobility, intrinsic concentration, impact ionization coefficients and generation/recombination lifetimes.

4.1. Influence of temperature on electron mobility

In the Philips unified mobility model, there are two contributions to carrier motilities. The first contribution represents phonon (lattice) scattering and the second one takes into account all other bulk scattering mechanisms due to free carriers, and ionized donors and acceptors. This electron mobility μ_{eff} depends on the doping density, and on the operating temperature. This temperature dependence can be expressed as [13]:

$$\mu_{eff} = g_s\left(\frac{1}{\mu_{lattice}} + \frac{1}{\mu_{impurity}}\right) \quad (3)$$

$$\mu_{eff} = g_s.\left(\frac{1}{\mu_{l0}\left(\frac{T}{300}\right)^{-2.2}} + \frac{1}{\frac{A.T^{1.5}}{N_A}\left[ln\left(1+\frac{BT^2}{N_A}\right)-\frac{BT^2}{BT^2+N_A}\right]}\right)^{-1} \quad (4)$$

Where g_s is represents the surface reduction factor due to the surface scattering effect and is equal to 0.5, A and B parameters depends on the doping density N_A, A and B are equal to $A=3,5.10^{1}(cmVS)^{-1}$,$B=1,52.10^{15}\ cm^{-3}K^{-2}$[13].

4.2. Influence of temperature on intrinsic concentration

Temperature dependant intrinsic concentration n_i is expressed as:

$$n_i(t) = \sqrt{N_c N_v}.exp\left(-\frac{E_g}{2kT}\right)$$

$$= \left[\frac{2\pi k\left(m_n^* m_p^*\right)^{0.5}}{h^2}\right]^{\frac{3}{2}} T^{\frac{3}{2}} exp\left(-\frac{E_g}{2kT}\right) \quad (5)$$

Where m_n^* and m_p^* are the electron and hole effective mass respectively, Eg is the silicon band gap (eV), h Planck's constant (Js) and k the Boltzmann's constant.

When the operating temperature increases silicon bandgap narrows, $n_i$increases, the related Fermi-potential and the depletion width in the device can also change.

4.3. Generation/Recombination lifetime

As cited above, the PD SOI n-MOSFET may be considered, as an association of a MOSFET transistor located in the top portion of thin film and a parasitic BJT located in the bottom portion of this thin film. For BJT transistors electron lifetime in the neutral region, generation lifetime and the recombination lifetime in the depletion region increases when the temperature increases affecting the leakage current of the device which increases as well.

The impact of the temperature variation on the cited parameters leads to drain current, threshold voltage and kink effect variation.

5. Results

Numerical simulation is an extremely helpful tool for detailed investigation of physical phenomena .It allows to determine the electrical characteristics of semiconductor devices. Technology Computer Aided Design (TCAD) is the most universally used simulation tools. Simulation results presented in this study had been performed using Atlas SILVACO Software [14].Thisdevice simulator offer many physical variables.

The main device parameters that influence the electrical behavior of our device are: its doping profile in and near the channel regions, the oxide "ε_{ox}" dielectric constant, oxide thickness "t_{ox}", the electrical gate length and gate work function, channel doping, source and drain doping, gate length L_G, length of source and drain junction . Actually, device simulator offers more variables, such as those used by physical models like mobility models simulator that influence strongly the electrical behavior of the device. The investigations provided in this work were carried out for an SOI n-MOS transistor; their extension to a P channel MOSFET device is straightforward. The starting point for our simulations is a basic structure represented in Figure2 and Figure3

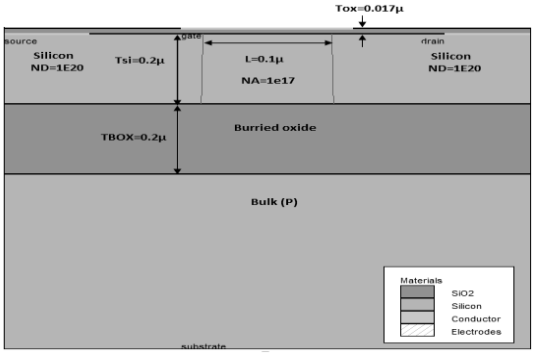

Figure 2. SOI n-MOSFET parameters.

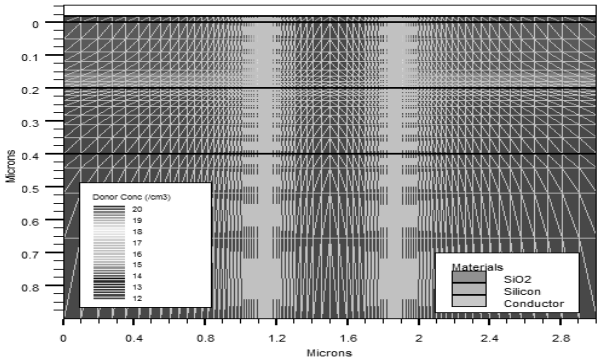

Figure 3. Device meshing

The different parameters of our SOI n channel enhanced transistor showninFigure 2are assumed as follows:

Drain and source length=1um, Gate length =1um, Channel length =1um, Gate oxide thickness t_{OX}=0.017um, Silicon film thickness t_{si}= 0.2µm, Buried oxide thickness t_{BOX}= 0.2um, Substrate doping =1x10^{17}cm^{-3}, Drain and source doping=1x10^{20}cm^{-3}. The structure shown in figures 2 is obtained for tsi= 0.2µm, that ensures a partially depleted channel. device meshing is shown in Figure3.

5.1. Influence of Silicon Body Thickness Variation on the Drain Current

Silicon film thickness is a key parameter, allowing designing a partially depleted or a fully depleted SOI MOSFET. In fact scaling silicon film thickness is desirable for better short channel behavior and reduced floating body effect. Consequently it is practical to consider the impact of silicon body thickness on the device performances. Figure 4(a) shows I_{DS}-V_{DS} characteristics for different silicon film thickness tsi.

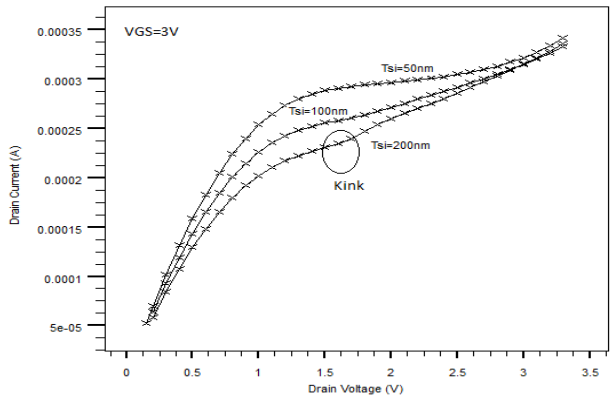

Figure 4(a). Output characteristics for different silicon film thickness tsi.

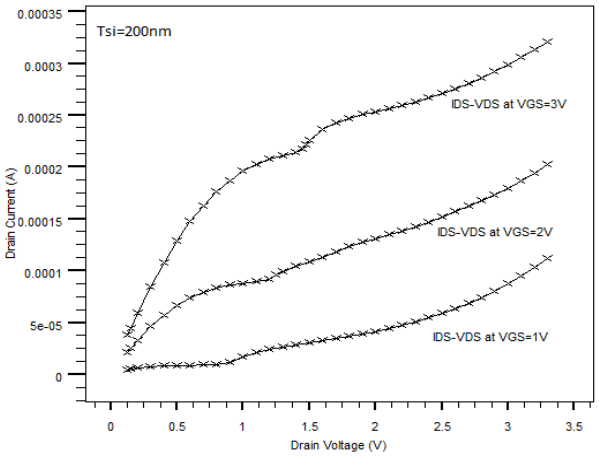

Figure 4(b) Output characteristics of the PDSOI n-MOSFET simulated.

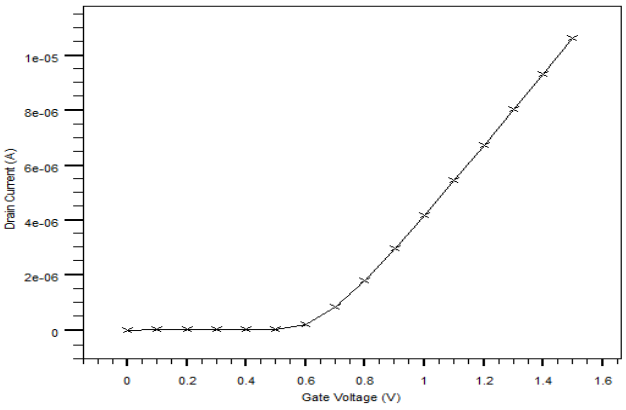

Figure 5. I_{DS}-V_{GS} characteristics of the PDSOI n-MOSFET simulated.

The output characteristics, shown in figure 4(b), exhibit a kink effect for a silicon body thickness equal to 0.2µ, essentially due to the floating body. In all the rest of our study, we maintain t_{si} value to 0.2µm. The I_{DS}-V_{DS} characteristics given in Figure 5 highlight a kink effect inherent in PD SOI transistors. The Presence of kink in these characteristics is clearly visible and belong to the so-called floating body effects. Depletion zone under the conducting channel does not extend sufficiently in-depth to reach buried oxide. Emergence of kink appears essentially for n-channel PD SOI MOSFETs above a certain value of V_{DS} voltage. At room temperature, Kink effect is not observed in bulk devices when substrate or well connections are provided, however kink effect can be observed in bulk MOSFET's operating at low temperatures. This effect is considered as the most important effects of the floating substrate, happening by the accumulation of carriers formed by impact ionization in the silicon film caused by high electric field near the drain region. In this case a part of the majority carriers which are

holes can migrate to the transistor body. This is principally due to the body potential V_B being firstly very close to V_S, that corresponds to zero. Whole migration leads to a local increase of V_B. If the voltage drop across the body-source diode is high enough, the junction may be switched, leading to a decrease of the transistor threshold voltage.We can also noticethat, in partially-depleted silicon thin-film SOI CMOS devices, due to the neutral region, an unsmooth transition in the drain current characteristics-kink effect is identified [15],[16].

5.2. Influence of temperature variation effects on the electrical characteristics of the device.

Knowing that SOI MOSFETs are conceived for applications where it is expected temperature variation or high temperature applications, we propose in this section to observe the impact of temperature variation on the electrical properties of our transistor.Typically, SOI MOSFET simulations are based upon the physical operation of the device, which exhibits both MOS and bipolar phenomena. As a result a more complex set of physical models will be required than for either MOS or bipolar technologies [14]. In order to study temperature variation effects, and based on
literature for SOI devices that have been intensively studies, , a set of typical models for a partially depleted SOI MOSFET have been used allowing taking into account the lattice heating (heat-flow). The numerical methods chosen for our simulations are Gummel and Newton methods.

5.2.1. Variation effects of the temperature on the PD-SOI n-MOSFET transfer characteristics

Figure 6, shows the simulated I_{DS}–V_{GS} characteristics for the simulated PD SOI n-MOSFET biased in the linear region (V_{DS} = 0.1V) and Figure 7 shows the same simulated characteristics in the saturation region (V_{DS}= 1.5V).

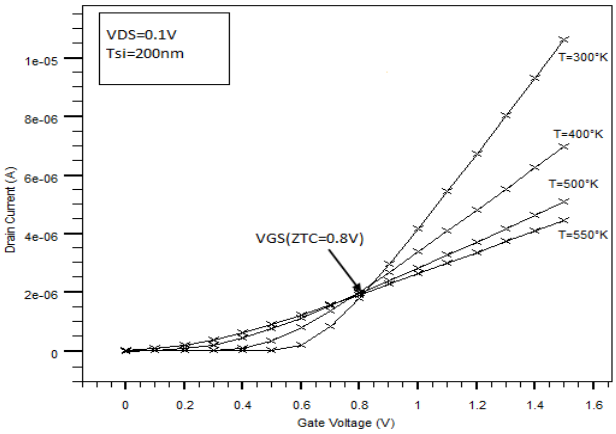

Figure 6. I_{DS}–V_{GS} transfer characteristics at differentoperating temperatures in linear region.

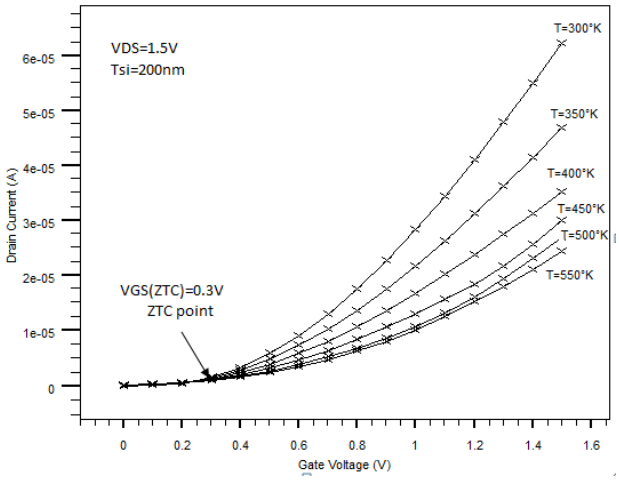

Figure 7. I_{DS}–V_{GS} transfer characteristics at different operating temperatures in the saturation region.

I_{DS}-V_{GS} plots allow extracting some electrical parameters of the structure such as the threshold voltage values. Our simulation results shown in Figures 6 and 7 highlight a particular V_{GS} voltage value for which the current is insensitive with the temperature fluctuation. In this significant operating point, the daring current is almost constant and independent of temperature variation. This common intercept point at different temperatures is called "ZTC point" a zero temperature coefficient bias [17]. Its existence can be explained by the fact that when the temperature increases, the threshold voltage decreases and V_{GS}-V_{TH}(T) term increases leading to I_{DS} increasing knowing that I_{DS} is proportional to V_{GS}-V_{TH}(T). At the same time, the mobility tends to decrease I_{DS} with temperature increasing for the reason that lattice scattering dominates at elevated temperatures leading to channel mobility diminution At low gate bias, V_{GS}-Vth(T) term dominates while at high gate bias, the mobility μ(t) term dominates.In summary we can say that the mobility tends to decrease I_{DS}, whereas the threshold voltage tends to increase this current. The consequence of this two temperature dependent parameters is the ZTC point. At this point the drain current is insensitive to temperature variation. Our simulation results allow us to note that V_{GS}(ZTC)=0.8V in linear region and V_{GS}(ZTC) =0.30V in saturated region. V_{GS}(ZTC) is lower in the saturation region. Biasing the transistor at V_{GS}(ZTC), leads to temperature independent behaviour. This property is use in some high performances applications. At theend of this section, we would like to recall a previous study developed by Shoucair, which helped to highlight the ZTC point of basic bulk MOSFETs .This ZTC point was up to 200°celsius [2].

5.2.2. Variation effects of the temperature on the PD-SOI n-MOSFET threshold voltage.

Threshold voltage variations with the operating temperature of our PD SOI n-MOSFET studied and extracted using ATLAS, are shown in Figure 8.

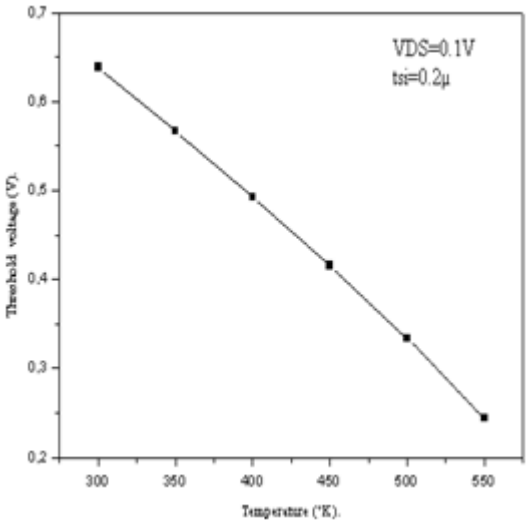

Figure 8. Variation of V_{TH} with operating temperature variation.

We can validate that V_{TH} decreases when the operating temperature decreases. In fact, threshold voltage temperature dependence comes from the energy bandgap, Fermi potential, and the depletion charge temperature dependence. The depletion charge temperature dependence is due to the Fermi potential dependence and Fermi potential temperature dependence is due to the temperature dependence of the intrinsic concentration ni, knowing that ni increases when the temperature increases while the Fermi potential and potential charge decrease lead to V_{TH} degradation [18].

5.2.3. Variation effects of temperature on the PD-SOI n-MOSFET transconductance "g_m" Characteristics.

Simulation results allowing observing temperature variation effects on g_m characteristics with the operating temperature of the partially-depleted SOI n-MOSFET device in a linear region are shown in Figures 9 and 10.

We can easily notice that the temperature has a direct impact on the gm-V_{GS} characteristics as shown in Figure 10. We can distinguish clearly, that for a weak inversion of the channel (V_{GS}< Vth,) the drain current is in fact attributable to diffusion and is known as subthreshold current .This leakage current increases with temperature increasing. Whereas for V_{GS}> V_{TH}, the channel is strongly inverted, this transconductance decreases with temperature increasing and this is mainly due to mobility degradation [19]. We can also observe, that a ZTC point can't be determined in linear region.

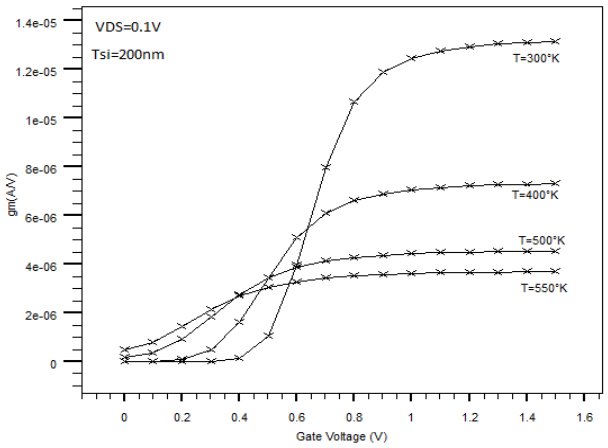

Figure 9. g_m-V_{GS} characteristics for the simulated PD SOI n-MOSFET at different operating temperature in the linear region.

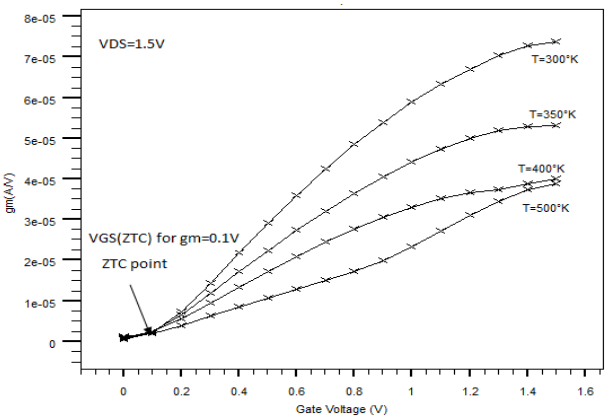

Figure 10. g_m-V_{GS} characteristics for the simulated PD SOI n-MOSFET at different operating temperature in the saturated region.

5.2.4. Temperature variation effects on the transistor output characteristics

Figure 11 exhibit the output plots for the simulated PD SOI n-MOSFET. These simulation results have shown the degradation of saturation current with rising temperature. At elevated temperature, the channel carriers mobility decreases due to lattice scattering leading to drain current reduction. It can also be noted that kink effect, principally due to holes generation accumulated in the neutral body as a result of impact ionization, is strongly reduced at high operating temperature as shown at T=400°K and 500°K.

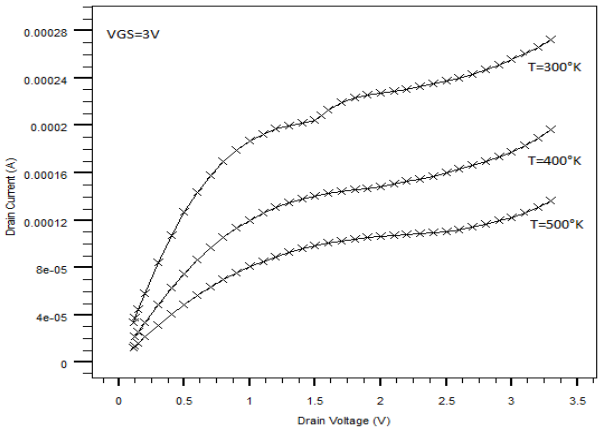

Figure.11. simulated output characteristics at different operating temperature.

5.2.5. Temperature variation effect on the transistor leakage current

A good comprehension of leakage current mechanisms in SOI CMOS technologies and leakage currents dependences on temperature is necessary in order to estimate the behavior of SOI CMOS technology for low-power circuits. The most important contributions to the off-state current in SOI MOSFETs are: the weak inversion current and the thermal generation current.

The cross section of SOI inverters and bulk CMOS inverters based on J.P.Colinge shown in Figure 12 and Figure 13 allow to illustrate the leakage components in SOI and Bulk technologies.

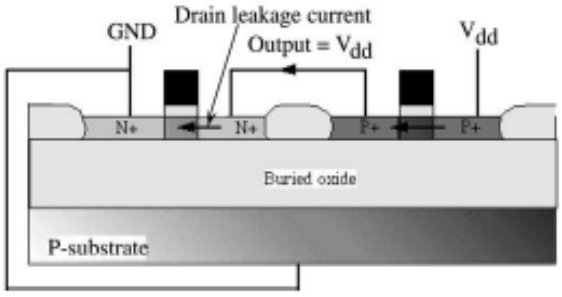

Figure 12. Cross-section of SOI inverters illustrating leakage components (based on Colinge) [11].

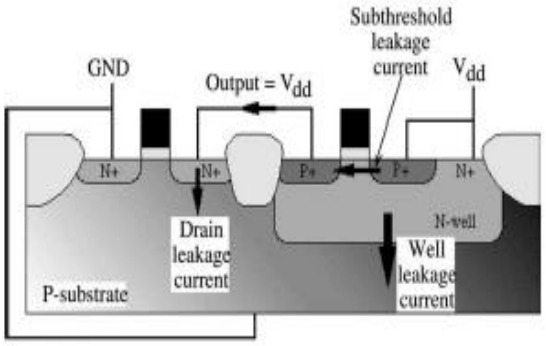

Figure 13. Cross-section of bulk CMOS inverters illustrating leakage components (based on Colinge) [11].

The OFF state current I_{OFF} is actually caused by thermal generation in the depletion region, in Bulk CMOS devices the most important source of thermal generation current shown in Figure 14 is the well junction that is more important than thermal generation at the drain junction, and this is mainly due to the large well area. In SOI devices, thermal generation current is reduced, and this lessening is due to the nonexistence of the well. As a general rule, the drain leakage current is 15–100 times smaller in SOI than in bulk MOSFETs [10]. However, in short-channel transistors, the weak inversion current becomes the most important contribution to off state leakage current in both bulk and SOI devices. This is essentially due to low V_{th}, necessary to maintain these short channel devices performances, and from Short channel effects leading to V_{TH} decreasing, and to subthreshold swing degradation that is smaller in SOI MOSFETS compared to bulk MOSFETS. Generally, a good device temperature behavioris needed and that because high performance SOI Integrated circuits are in fact conceived in order to operate at high temperature.However, it is found that off state

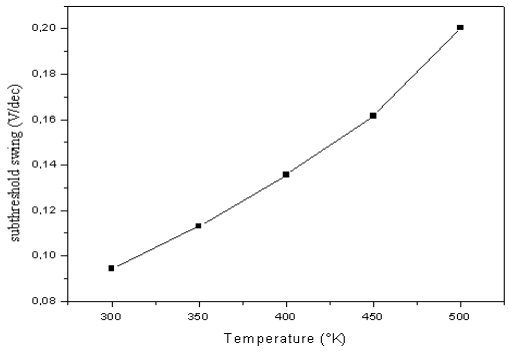

Figure 14. Subthreshold voltage variation with operating temperature variation.

leakage current increases when the temperature increases and this principally due to V_{TH} decreasing with operating

temperature increasing as shown in Figure 8. Subthreshold swing also increases with temperature increasing as shown in Figure 14 leading to the off state current increases.

Figure 15 and Figure 16 shown log I_{DS}-V_{GS} curves at operating temperature of 300,350,400, 450,500 and 550°K in both saturation and linear region. These simulations results we obtained allow investigating the temperature variation effects on the off state current of our device. As expected, the I_{off} leakage current increases with temperature increaing, both in linear and saturated region, and this was perfectly predictable.

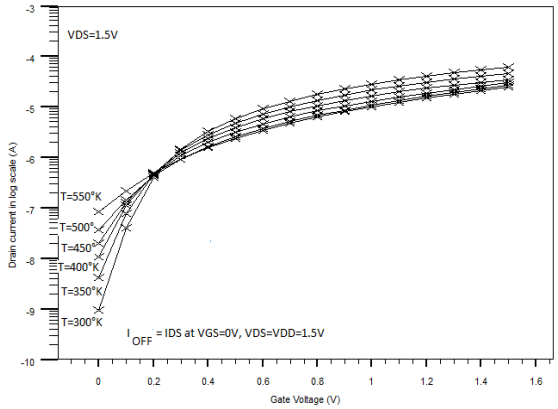

Figure 15. Temperature variation effects on the off state current for a partially depleted SOI n-MOSFET: in the saturation region (V_{DS}=1.5V).

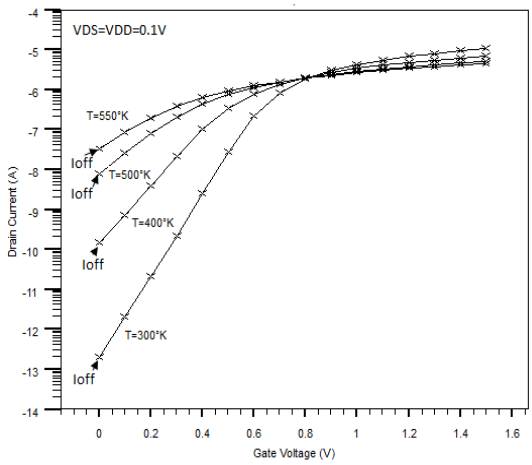

Figure 16. Temperature variation effects on the off state current for a partially depleted SOI n-MOSFET in linear region (V_{DS} =V_{DD}= 0.1V).

At the end of this section, we can affirm that the off state current increase with temperature is less significant in SOI CMOS technologies than in bulk CMOS and this is mainly due to: the lower dependence of the threshold voltage on the temperature for SOI devices, the better value of the subthreshold, the reduced short-channel effects, and the absence of well junctions for SOI devices [20].

5.3..Self heating effects

It is well known thatSOI devices exhibit self heating effects. Self heating effects arise because SOI devices are thermally insulated from the substrate by their buried oxide layer, leading to a significant elevation of temperature within the SOI device, which accordingly modifies the output characteristics of the device.

Self heating effects that have an important effect on drain current must be taken into accountt by device technology designers. In this work, tthermal and electrical effects are coupled through self-consistent calculations.

In Figure 17 the temperature distribution within our PDSOI n-MOSFETis shown. We can observe that the thin film's temperature appears to be upper than the external temperature that is room temperature T=300°K.

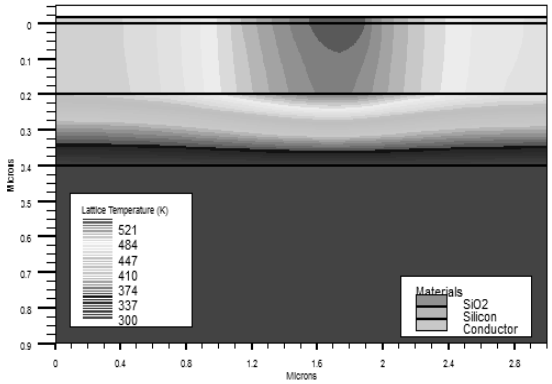

Figure 17: Temperature distribution within a partially depleted SOI n-MOSFET. External temperature is equal to 300 K.

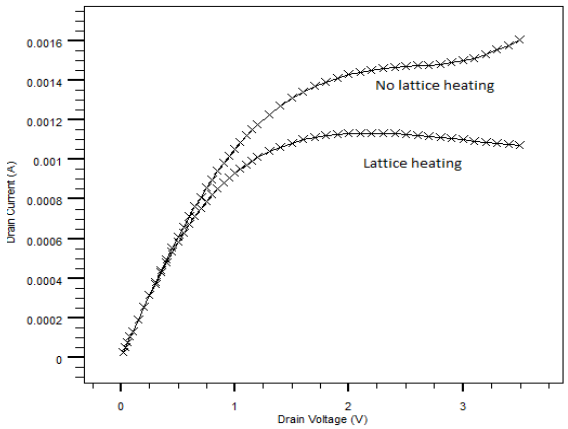

Figure 18. I_{DS}-V_{DS} with lattice heating and isothermal models.

Simulation results shown in Figure 18 allow comparing I_{DS}/V_{DS} curves for our SOI transistor using isothermal and non-isothermal approaches. We can observe that heating of silicon film causes a negative saturation slope.
that can be explain by the fact that at high temperatures, lattice scattering dominates and causes a carrier mobility reduction leading to drain current decreasing. Basically self-heating effects are more pronounced under higher drain and gate biases.

6. Conclusion

In this paper, all the device parameters considered in our investigations are fully simulated using SILVACO Atlas device simulator. The numerical simulation results, we obtained and relating to temperature variation effects on the electrical properties of partially depleted silicon on insulator n-channel MOSFET, are presented. Based on our results, we can conclude that the temperature has a significant impact on the device behavior. Our first conclusion was that kink effect in PD SOI n-MOSFET is strongly reduced at high operating temperaturedue to holes generation accumulated in the neutral body, as a result of impact ionization.Concerning the effects of temperature variation on the electrical characteristics of our device, we observed that the threshold voltage, the mobility and the drain current decreased when the operating temperature increased. This study also allowed us to highlight a bias point called ZTC point, where the drain current and transconductance show no temperature variations and to observe that ZTC point exists in both the linear and the saturation regions. In this study we have observe the temperature variation effects on the off state current of SOI MOSFETS. The I_{off} current of our device increases as the temperature increases, however, the off state current increase with temperatureremains very weak and is smaller in SOI CMOS technology than in bulk CMOS technology. At the end of this work self heating effects that affect the drain current in its saturation region, causing the Ageing of the device have also been presented.

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Voice Recognition Technology Using Neural Networks

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Abstract

This paper presents the use of a Multi-Layer Perceptron Neural Nets (MLP-NN) for voice recognition dedicated to generating robot commands. Our main goal concerns the estimation of the minimal number of elements required for the learning process in order to ensure an acceptable success of the neural nets recognition system. As the MLP requires references for the spoken words, we have provided these references by the means of a supervised classifier based on the mean square error.

An experimental approach has been followed for the design of experiments enabling to determine the minimal elements in the sample for each voice command. Satisfactory results have been obtained leading to a better understanding of variability of the system functioning. Finally, we have noticed that the success rate of the MLP and the minimal number of elements used for the learning process depend on the spoken word structure and of the variability of the situation (word length, noise, speaker, etc).

Keywords:design experiments, MLP, neural networks, speech recognition, supervised learning, VQ-LBG algorithm;

1. Introduction

Speech recognition is an important tool for control and interaction with modern robots. However, because of the complex nature of voice signal, the speech recognition still remains a hard issue. Most speech recognition systems use a learning process to identify the correct response of a spoken command. In this context, an interesting issue concerns the design experiments to reduce the data used for the learning phase. Compared to the design experiments in the case of discrete data, NN Model can be used for estimating the output of nonlinear systems in the case of noisy and sensitive process to various parameters such as speech recognition.

The field of automatic speech recognition (ASR)[1]is divided into four areas: recognition of isolated words recognition of chained words, continues recognition and speech understanding with a limited vocabulary and syntax. For our application; we are concerned with the recognition of isolated works that will be used as robot commands. [1].There exist different methods of speech recognition of isolated words using methods such as Hidden Markov Model [2,3], the Gaussian mixture models, VQ vector quantification [4,5],and NN(MLP)[6,7], etc. Concerning, the NN, we have remarked the use of self organizing Map[8], Waibel's Time Delay NN [9], Perceptron and Recurrent NN [10]. The multilayer Perceptron (MLP) is of a particular importance for acoustic modelling in ASR [7].

On the other hand, a survey of literature related to applications of NN applied to design experiments shows that they can be used to model complex non-linear and noisy processes[11,12].

In this paper, we intend to exploit MLP-NN for design experiments in order to determine the minimal number in a sample to reducing the data, time and cost used for the learning phase process[13]. The estimation of the reference words (robot commands) are obtained by a supervised classifier based on the minimization of the mean square error. These references words are stored into the dictionary and

used by the MLP to compare a pronounced word with a desired one.

We have tested this type of commands for a various kind robots including: mobile robot, serial robot manipulator and cable based robot.

2. The Initial Word Recognition System

The principle used for most Word recognition Systems can be illustrated in figure 1. It comprises two phases: the recognition phase and the learning phase. The learning phase consists of creating a list of words which are stored into a dictionary as reference words. The recognition phase consists of identifying a spoken unknown word to one of the reference words stored in the dictionary[14].

We have implemented a word recognition system based on the following procedure: Any spoken word which is a continuous acoustic signal is translated by the microphone into an electric continuous signal.
This continuous electrical signal is then digitalized (sampled) by the sound card. Some digital operations are applied such as pre-emphasis, short-time Fourier analysis (FFT), power spectrum, filter bank integration (Mel's Filter), logarithmic compression, Discret Fourier transform. Some of these operations are applied to the spoken word START as shown in Figure 1. In this Figure 1-a represents the spoken word converted into an electrical signal by the microphone.
Figure 1-b represents the positive envelope of the electrical signal. Figure 1-c represents the detection of amplitude variation of this signal as on-off levels. Figure 1-d represents the detection of beginning and end of the spoken words.
The final output is a set of coefficients which are called Mel frequency Cepstral coefficients MFCC.The MFCCis technique to extract features from thespeech signal and compare the unknown words with some reference words stored in a database.
TheMFCC are based on the known variation of the human ear'scritical bandwidth frequencies with filters spaced linearly atlow frequencies and logarithmically at high frequencies usedto capture the important characteristics of speech. Studieshave shown that human perception of the frequency contentsof sounds for speech signals does not follow a linear scale.Thus for each tone with an actual frequency, *f*, measured inHz, a subjective pitch is measured on a scale called the Melscale. The Mel-frequencyscale is linear frequency spacingbelow 1000 Hz and a logarithmic spacing above 1000 Hz. Asa reference point, the pitch of a 1 kHz tone, 40 dB above theperceptual hearing threshold, is defined as 1000 Mels[15].
Vector quantization (VQ) is a lossy data compression method based on the principle of block coding. It is a fixed-to-fixed length algorithm. In the earlier days, the design of a vector quantizer (VQ) is considered to be a challenging problem due to the need for multi-dimensional integration. In 1980, Linde, Buzo, and Gray (LBG) proposed a VQ design algorithm based on a training sequence. The use of a training sequence bypasses the need for multi-dimensional integration. A VQ that is designed using this algorithm are referred to in the literature as an LBG-VQ [16]. The algorithm requires an initial codebook$C^{(0)}$. This initial codebook is obtained by the fractionation method (splitting) .In this method, an initial code vector is set as the average of the entire training sequence. This code vector is then split into two. The iterative algorithm is run with these two vectors as the initial codebook. The last two code vectors are divided in four and the process is repeated until the desired number of code vectors is obtained [14].

We used the VQ-LBG to reduce MFCC data from (12*128) to (12*32) coefficients. Figure 2 shows the electrical form of the spoken word START as well as its representation as MFC Coefficients and their compression into centroids[14].

The estimation of the reference words (robot commands) are obtained by a supervised classifier based on the minimization of the mean square error. These references words are stored into the dictionary and used by the MLP to compare with a pronounced word.

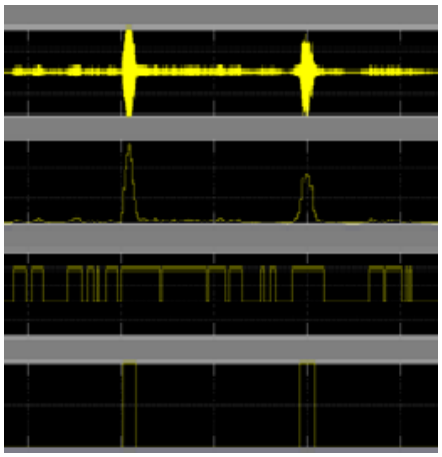

Figure 1: steps and procedure of treatment and detection of each spoken word

Figure1 represent an example of application implemented under matlab software.

3. MLP for Word Recognition

The technique of NN is used in several areas such as classification, pattern recognition (image, voice, ect.) and process control. In our work, we replaced the classifier by an MLP for voice recognition [11, 17,18].

The role of the MLP classifier is to select the most similar reference word with respect to an unknown word. The choice is based on the calculation of the distance between the unknown word and all the reference words (nearest neighbor) [17,7]. The scheme of a voice recognition system is given in Figure 2.

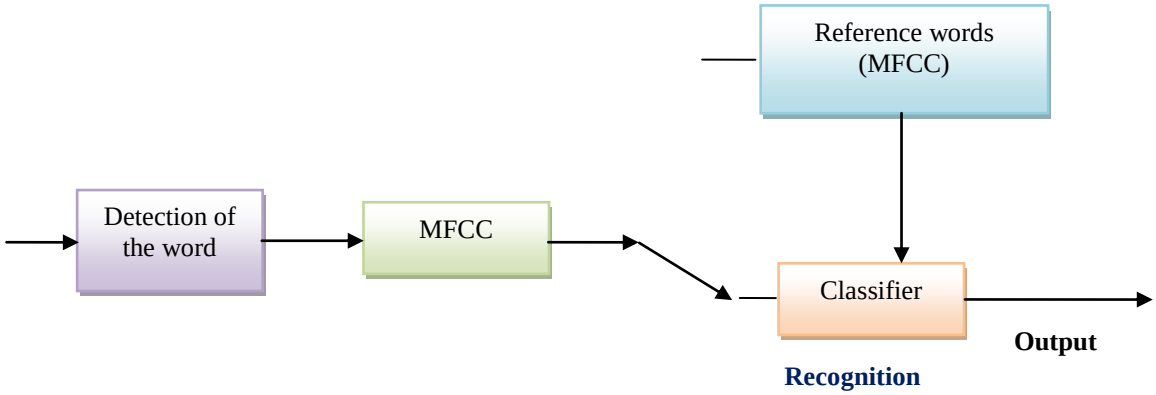

Figure 2: Voice recognition system

For our speech recognition system, we have chosen an FFT resolution of 1024 points. The result is an MFCC coefficients matrix of dimension $12 \times j$, where the value of j depends on the length of the spoken word, on the sampling frequency of the sound card and on the resolution of the FFT. The system is tested on a dictionary of four commands (START, STOP, UP, DOWN). The MFCC matrix is compressed into a The MFCC matrix is compressed into a matrix of (12×32) centroid coefficients. For the given commands;
We have the following dimensions (Table1):

Command	MFCC	MLP
START	12×128	12×32
STOP	12×128	12×32
UP	12×128	12×32
DOWN	12×128	12×32

Table 1: Dimensions Matrix of MFCC and MLP inputs

The implementation of the MLP was carried out by using the NN toolbox of Matlab software. Our MLP is a NN format; it is composed of an input layer and an output layer with one hidden layer in between (Figure 3). The input data of the MLP are the MFCC which are recorded into a file in a form of a matrix named "sepstr.mat". The MLP uses 12*32 neurons for the input layer.

The reference word was determined from the previous process. A supervised training was adopted comparing actual spoken words with those stored on the dictionary. After the achievement of the learning process, the obtain hidden layer derived from Matlab tool is constituted of 32 neurons.

The output layer is constituted of 4 neurons which corresponds to the reference words stored on the dictionary (START, STOP, UP, DOWN).

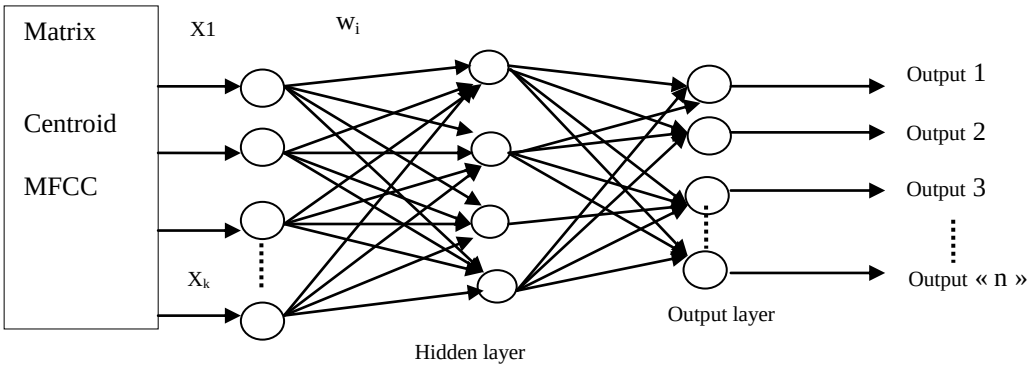

Figure 3: MLP voice recognition system

4. Experimental Results

It is important to analyze the evolution and the convergence of the learning process with respect to the number of experiments. To get an estimation of the required minimal number of elements in a learning tests for a given reference word during the learning phase; we have adopted an experimental approach. This leads to reduce the computation time.
Under Matlab software, the learning phase for the MLP was tested as follows. Each learning test corresponds to a certain number of trials N of learning experiments using the same word. For each reference word, the mean square error of MFCC is computed with respect to the number of trials N as

$$mse(N) = \frac{\Sigma(a_{ij}^{*} - a_{ij})^2}{N}$$ using the same word.

For different learning test, the mse(N) is recorded.
On the other hand, we have applied various approximations functions in order to obtain an appropriate form of the evolution of the learning process. As a result, we have noticed that the most appropriate approximation of the learning process is a bi-exponential function in the form of: f(x) = a*exp(b*x) + c*exp(d*x).

We present graphically two examples illustrating the learning process. The first example shows the evolution of the learning process with respect to the number of trials for the word STOP. Figure 4-a shows the electrical signal of the word STOP. Table 2 shows the experimental results of 9 learning tests
with respect to the number of trials for the word STOP.
As shows in Figure 4-b, the analysis of these experiments shows that the mse(N) decreases with the number of trials; improving therefore the learning process.
For the example at hand, the bi-exponential approximation function is given by the Curve Fitting toolbox of Matlab Software as:f(x) = a*exp(b*x) + c*exp(d*x) with the following coefficients:
a = 2.019e+004 (-2.852e+014, 2.852e+014)
b = -0.0634 (-5413, 5413)
c = -2.019e+004 (-2.852e+014, 2.852e+014)
d = -0.0634 (-5413, 5413)
(with 95% confidence bounds), Goodness of fit: SSE(0.01536), R-square(0.984),Adjusted R-square(0.9787), RMSE(0.04131).

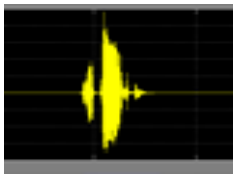

Figure4-a: example of the spoken word STOP

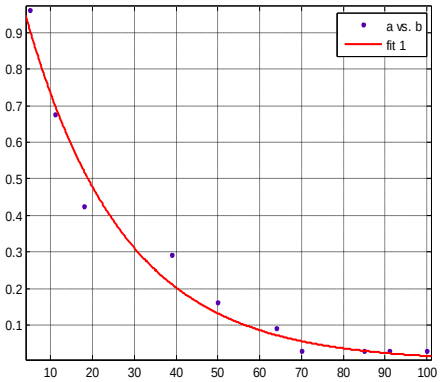

Figure 4-b: word STOP Error distribution with the growth in the number of test

The second example concerns the training process for identifying the word UP with respect to the number of trials. We have used 10 learning tests. As shows in Figure 5, the analysis of these experiments shows that the mse(N) decreases with the number of trials,

Learning tests	mse(N)	N (trials)
1	0,9094	10
2	0,3313	23
3	0,1686	36
4	0,1195	41
5	0,0674	54
6	0,0490	56
7	0,0244	61
8	0,0209	59
9	0,0191	60

Table2: Experimental learning tests mse(N)

the bi-exponential approximation function is given by the Curve Fitting toolbox of Matlab Software as the following coefficients:
General model:Exp2: f(x) = a*exp(b*x) + c*exp(d*x)
a =2.073e-008 (-6.453e-006, 6.495e-006)
b =0.1348 (-3.013, 3.282)
c =1.129 (0.9298, 1.329)
d = -0.04309 (-0.05608, -0.03011)
(With 95% confidence bounds), Goodness of fit: SSE: 0.02093, R-square: 0.9778, Adjusted R-square: 0.9667, RMSE: 0.05906

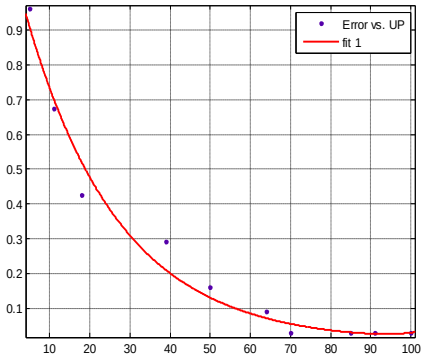

Figure 5: Word UP Error distribution with the growth in the number of test

After testing experimentally the MLP with some spoken robot commands (START, STOP, UP, DOWN), We have remarked that this minimal number depends on the structure of the spoken word itself, on the speaker, on the used equipment and on the environment noise.

We can also notice promising results while testing this type of commands for various kind of robots such as those experimental systems developed in our laboratory including: mobile robots, serial robot manipulators and cable based robots.

5. Conclusion

We have presented an experimental technique for design experiments to estimate the minimal number that should compose a learning test to ensure an acceptable performance for a learning process of supervised neural networks dedicated to speech recognition used for robot commands.

We have initially developed a system of word recognition based where any spoken word is processed and translated into a set of coefficients which are the Cepstral coefficients (MFCC). Then, these MFCC coefficients are compressed to centroids by the VQ-LBG algorithm based on the mean square error.

Neural networks are a technique to analyze and make an estimate of the output of a nonlinear system in the case of a random process. However; the MLP requires reference words. For each spoken word, its reference has been obtained by calculating the mean value of its MFCC Centroids Coefficients. These reference words have been used as words models to train a supervised learning NN of type MLP.

We have experimentally tested the MLP with some spoken robot commands and we have obtained an estimation of the required minimal number of elements in a learning test to ensure an acceptable learning process. We have remarked that this minimal number depends on the structure of spoken word itself, on the used equipment and on the environment noise. We have remarked that we can approximate the learning process by a bi-exponential function.

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A study of C(V) characteristics of capacitors containing high-k oxides and high mobility carriers semi-conductors.

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Abstract

In this work, we proceeded to the analysis of C(V) characteristics of MOS capacitors (Metal-oxide-semi-conductor) with metal gates.

Within the framework of the search for new materials, we have studied C(V) characteristics of structures containing high permittivity oxide (high-k)- the HfO_2 in our case- to replace the ultra-thin conventional oxide layer (SiO_2) which reaches its physical and technological limits (less than 1 nm thickness).

In these same structures, the stacking of grid is deposited on a substrate with high mobility carriers (electrons and holes). In fact: The germanium (Ge) and III-V materials [1].

The obtained results were largely compared with others simulated and experimental ones.

Keywords: MOS capacitors, C(V) characteristics, High permitivity, high mobility carriers, Schrodinger.

1. Introduction

The micro-electronics industry succeeded in developing the MOSFET transistor as well as the circuits which integrate it, this is in order to satisfy society requirements.

This spectacular developpement is essentially caused by the concept of the miniaturization based on the reduction of all component's dimensions, particularly, channel's length and oxide's thicknesses.

However, this reduction is never without fatal consequences on the behavior of these miniature components.

In fact, several parasitic effects take place and degrade clearly the component's behavior, especially, leakage currants through the oxide layer [1, 2, 3].

For this reason, new alternatives are explored in the framework of the search for new materials and new architectures, used to cure these problems, and then, to improve components performances.

In this context, this present work shows the famous performances of the basic structure of all MOS technology components. In fact: The MOS capacity, having the double-layred (HfO_2 / SiO_2) as a grid oxide, which is deposited on a substrate with high mobility carriers semi-conductors [1, 4].

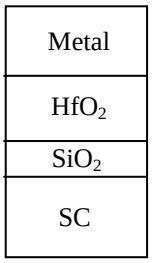

Fig.1: *Presentation of the studied structure containing High-k oxide*

For that, we proceeded to obtaining C(V) characteristics of the MOS structure described above, and this, by resolving the coupled « Poisson » and « Schrodinger » equations, this resolution was done numericaly, using Newton-Raphsson iterative method [3].

2. The role of the High-k gate oxide in new structures:

The principle is then to replace the ultra thin layer of (SiO_2) conventional oxide, by another thick layer of high-k oxide. Theses capacities are electrically equivalent, but the structure containing high-k oxide

constitutes a good remedy to leakage currents problems. In real structures, oxide layer results from the native oxidation of the substrate surface during its deposit. The following figure is more explanatory [5]:

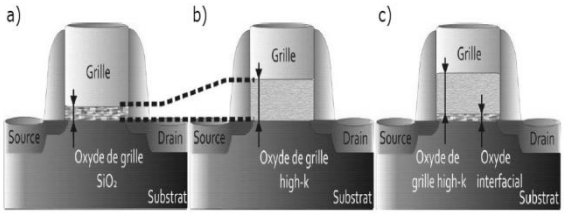

Fig.2: (a) : Conventional oxide . (b) : Integration of High-k oxide. (c) : Real structure

In this case, we can't speak of oxide thickness, but rather, of the equivalent oxide thickness EOT (Equivalent Oxide Thickness) given by the following expression [1, 5]:

$$EOT = t_{SiO2} = (\varepsilon_{SiO2} / \varepsilon_{High\text{-}k})\ t_{High\text{-}k}$$

Then, with a larger physical high-k oxide thickness, and equivalent electrical characteristics, the leakage current is strongly reduced involving an increase of the ratio I_{ON}/I_{OFF}, which is so beneficial for MOSFET transistors.

3. Equations and numerical details:

Obtaining C(V) characteristics requires then the self-consistent resolution of the following system [3] :

$$\begin{cases} \dfrac{d}{dx}\left(\varepsilon_0\ \varepsilon_{si}\ \dfrac{d}{dx}\right)\phi(x) = -q\left[p(x) - n(x) - N_A^-(x)\right] \\ -\dfrac{\hbar^2}{2}\dfrac{d}{dx}\left(\dfrac{1}{m^*}\dfrac{d}{dx}\psi_i(x)\right) + V(x)\ \psi_i(x) = E_i\ \psi_i(x) \end{cases}$$

Where ε_{si} is (Si) dielectric constant , Φ (x) is the electrostatic potential, $N_A^-(x)$ is ionized acceptors concentration, n(x) and p(x) are respectively free electrons and holes concentrations, ħ is the reduced Plank constant, m^* is electron effective mass, E_i et ψ_i are respectively, the confinement energies in the quantum well and equivalent wave functions . (x) is the spatial coordinate.

We point out that « Schrodinger » equation allows to model quantum phenomena which appear under the oxide – at the interface (ox/sc) -. Indeed, the small thickness of used oxides and the high doping levels, cause a strong electric field at the substrate surface, which makes curve the energy bands (conduction and valence) at the surface [6]. A quantum well is then created, carriers are confined into and are assimilated to a two-dimensional gas, their movement is free in the plan of the structure but confined in the perpendicular one [2, 5].

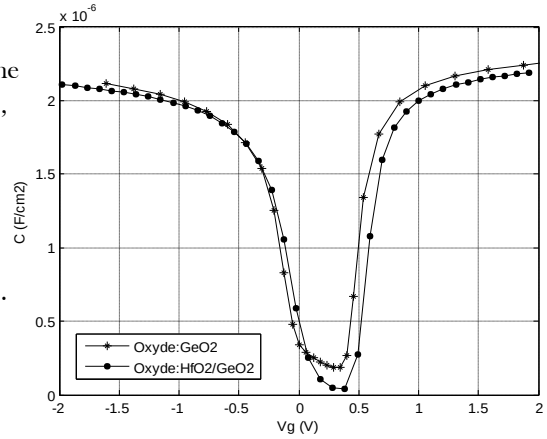

Fig.3: One layer oxide GeO_2. Bi-layer oxide HfO_2/GeO_2

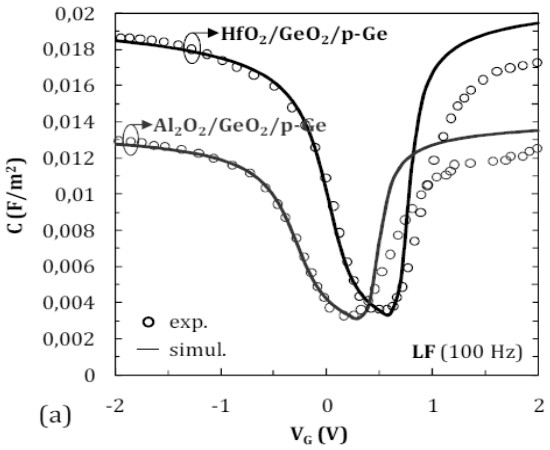

Fig.4: Structure with bi-layer oxide: HfO_2/GeO_2 [1,4]

4. Modeling of C(V) characteristics :

The resolution of the coupled system presented below, provides us carrier concentrations (electrons and holes) and also, the electrostatic potential in each mesh point of the structure, and this, for each applied oxide bias.

The total potential applied to the gate (V_g) is then calculated via the following expression [7]:

$$V_g = V_{ox} + V_{FB}$$

Where V_{FB} is the flat band potential [5] :

$$V_{FB} = \Phi_M - (\chi + Eg/2 + Efs)$$

- Φ_M is the work function of the metal gate.
- χ, Eg and Efs are respectively the electronic affinity, the bandgap and

the Fermi energy of the semi-conductor.

The capacitance is then obtained by differentiating the total charge in the substrate and the gate bias according to the expression [3]:

$$C = \Delta Q / \Delta V_g$$

5. Results

5.1. Interest of high permittivity oxides :

We simulated the C(V) characteristics of a capacitor with a bi-layer oxide (t_{HfO2} = 4 nm et t_{SiO2} = 1.4 nm), which corresponds to an equivalent oxide thickness of EOT=2.3 nm approximately. This stacking being deposited on a (Ge) substrate doped (P) at $10^{17}cm^{-3}$, the gate metal having a work function of 4.6 ev.

The (Fig.3) represents C(V) characteristics of the two structures presented bellow, it shows clearly that they are electrically equivalent. That containing High-k stacking, has in additional, the advantage of decreasing leakage currents because of its physical thickness relatively large.

Our C(V) are very comparable with those simulated by [1,5].

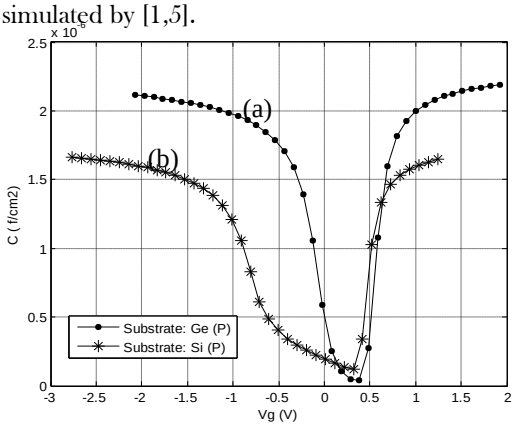

Fig.5: Bi-layer HfO_2/GeO_2 (a). Bi-layer HfO_2/SiO_2 (b)

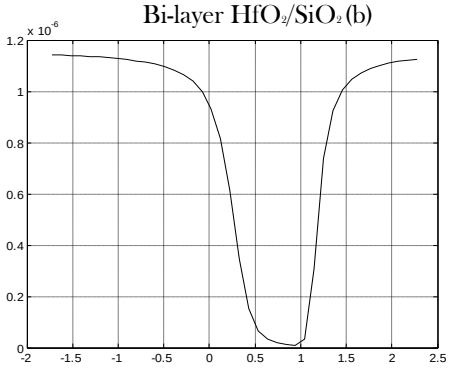

Fig.6: C(V) curves of a structure with GaSb substrate

5.2. Influence of substrate with high mobility carrier:

- *Germanium (Ge) substrate:*

We simulated in this time, the C(V) characteristics of two different capacities : the first one having the bi-layer oxide (HfO_2/GeO_2) deposited on a Ge(P) substrate, while the second one is constituted of the bi-layer oxide (HfO_2/SiO_2) deposited on a Si(P) substrate.

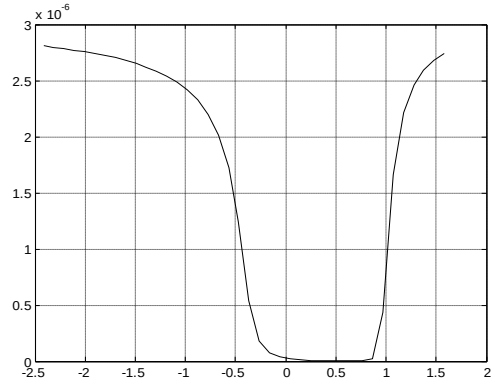

Fig.7 : C(V) curves of a structure with GaAs substrate

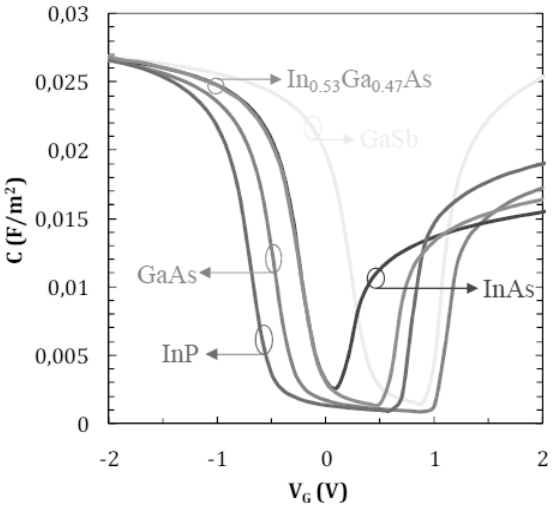

Fig.8 : C(V) Curves with substrates in different III-V materials simulated by [1]

The introduction of High-k oxides in new structures is always accompanied by an interface states density, which tends to trap free carriers and then, to decrease the drain current in transistors. For this reason, a radical change of the substrate material was considered. Indeed, materials with high mobility carriers cure rather well trapping problems.

In the other part, Germanium (Ge) with its small bandgap with respect to that of Silicon (Si), ensures a short depletion region in term of gate voltage. The passage from the accumulation to the

inversion mode, is then so rapid, this is clearly shown on the (Fig.5).

- *Substrate in (III-V) materials :*

(Fig.6) and (Fig.7) represent C(V) curves obtained for structures containing (III-V) materials, respectively : The (GaSb) and the (GaAs), they confirm in their turn that the speed of the passage from accumulation to inversion mode is directly related to the smallest bandgap ($E_{g\,(GaSb)} < E_{g\,(GaAs)}$).

These results are also in a good agreement with those obtained by [1] (Fig.8).

6. Conclusion

In this paper, we presented a work which permits us to highlight the interest of high permittivity oxides integration in new generations of MOSFET transistors.

Indeed, these High-k oxides permit obtaining the same electrical properties of capacitors containing ultra-thin oxides, but by using physical thicknesses relatively large. This will largely cure leakage currents, which exceed 1A/cm^2 for t_{SiO2} thickness of about 1nm.

Also, using substrates containing high mobility carriers is a good solution to counter the effect of carriers trapping by the interface states appearing during the integration of high-k oxides.

The obtained results show clearly the substrate band gap effect on the depletion region, this effect describe the commutation from accumulation to inversion mode and decides then of transistors drain current.

Our simulated results are in a very good agreement with other simulated and experimental ones obtained by other authors.

This permits us to validate our simulation code and proves its efficacy.

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Design and simulation of MATLAB / Simulink. Influence of external and internal parameters of photovoltaic cells

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Abstract

This article is devoted to the simulation of a model of a single photovoltaic cell described by mathematical equations comprises a photoelectric generator, a diode, a series resistance and shunt resistance. The goal is to draw IV and PV characteristics under Changes five parameter, external (temperature settings, illumination) and internal (series resistance, shunt resistance, factor ideality and the saturation current) and the influence of each parameter on the model.

Keywords: photovoltaic cell, MATLAB Simulink, characterization, modeling, electrical parameters.

1. Introduction

The principle of the photoelectric effect (Direct transformation energy from light into electricity) was applied in 1839 by Antoine Becquerel and his son Edmond Becquerel who noted that a chain of elements conduct electricity gave to a current spontaneous electric when she was enlightened. [1].
Later, selenium and silicon (which finally for reasons of cost supplanted cadmium-tellurium or cadmium-indium-selenium also tested) were shown capable of producing the first cells photovoltaic (exposure meters for photography soon 1914, and 40 years later (in 1954) for an electricity production). Research also carries today on organic polymers and materials (possibly flexible) which could replace silicon. [1]

2. Photovoltaic module Msx60

The photovoltaic cell is made of a material semiconductor that absorbs light energy and transformed directly into electric current [2] [3] [4] [5].

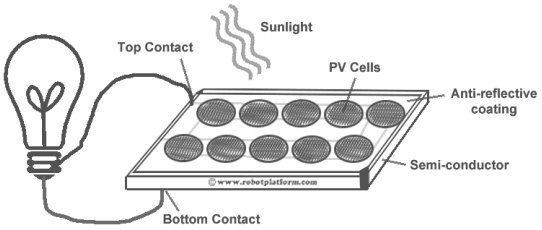
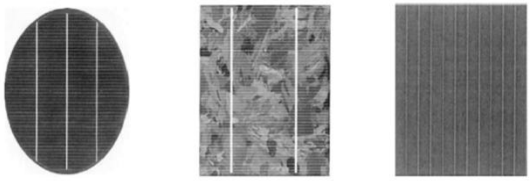


Fig.1: The principle of solar cell work

The different cells PV according to their performance are:

2.1 Mono-crystalline cell [2] [3] [4]
Mono-crystalline silicon cells are formed a silicon single crystal.
2.2 polycrystalline Cell
Cells in polycrystalline silicon are formed of several silicon crystals.
2.3 Amorphous Cell
The amorphous silicon cells made with amorphous silicon, not crystallized, spread on a plate of glass.
2.4 Tandem cell
There are also other types of cells, such as tandems, consisting of several cells and cells in plastiques.



Mono-crystalline *Polycrystalline* *Amorphous*

Fig.2: types of PV cells [6]

The following table shows the different cells PV according to their performance:

Technology	Efficiency	Efficiency	Efficiency
Mono-crystalline	24.7	21.5	16.9
polycrystalline	20.3	16.5	14.2
Amorphous	13	10.5	7.5

3. Modelling of the photovoltaic cell

An evaluation of the operation of PV modules and design of the power systems is based on the electric current-voltage characteristic of the cells and PV modules. The modelling of these generators can be

performed by means of equations which provide different degrees of approximation to the real device. In this article exponential model of the PN junction was chosen for the PV cell. Fig.1 shows the circuit equivalent. This circuit requires five parameters are known: enlightenment, the current Iph, the current reverse saturation of the diode, the series resistance Rs and shunt resistance Rsh [6] [7] [8] [9].

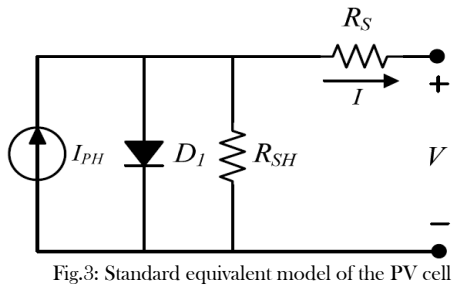


Fig.3: Standard equivalent model of the PV cell

The equation that describes its behavior to temperature and fixed solar radiation [1-13]:

$$I = Iph - Is\left(exp\left(\frac{V+RsI}{a}\right) - 1\right) - \frac{V+RsI}{Rsh} \quad (1)$$

For irradiation and temperature data, equation (1) has different combinations of a, Rs and Rsh allowing passage near the same points ISC, IM, VM and VOC curve I-V. Taken separately, these values of a, Rs and Rsh only are not appropriate. What really makes the significant is the ratio consisting of three parameters.

The relationship of power for a module PV is given by:

$$P = IV \quad (2)$$

Thermal voltage is expressed by:

$$\boldsymbol{a} = \frac{\boldsymbol{NsKT}}{\boldsymbol{q}} A \quad (3)$$

Where:

q: elementary charge 1,607 10 -19 C
A: coefficient of ideality of the cell; it depends on the material.
K: Boltzmann's constant = 1.380 10 -23 J / K
T: temperature in degreesKel
Rs: series resistance of the cell (Ω).

Rsh: shunt resistance (Ω).

NS :the number of series connected cells.

Applying the short-circuit conditions in equation (1),

Iph is obtainable by:

$$\text{Iph} = \text{Isc}\left(1 + \frac{Rs}{Rsh}\right) + Is(exp\left(\frac{Rs}{Rsh}\right) - 1) \quad (4)$$

Equations (3) and (4) induce

$$\text{Is} = \frac{\text{Isc}\left(1+\frac{\text{Rs}}{\text{Rsh}}\right)-\frac{\text{Voc}}{\text{Rsh}}}{\exp\left(\frac{\text{Voc}}{\text{a}}\right)-\exp\left(\frac{\text{IscRs}}{\text{a}}\right)} \quad (5)$$

exp (Voc/a) >>exp (Isc.Rs/a), equation (5) is simplified in:

$$Is = \left(Isc - \frac{Voc}{Rsh}\right) exp(-\frac{Voc}{a}) \quad (6)$$

ISC and Voc represent respectively the current short circuit and open circuit voltage..

4. Photovoltaic module Msx60

We chose a mono-crystalline silicon cells module composed of 36 Msx60 with a maximum power of 60connected in series .W is considered in standard conditions G = 1000W / m2, T = 25 ° C. To realize the modelling of this module, we used MATLAB as a tool for testing and simulation.

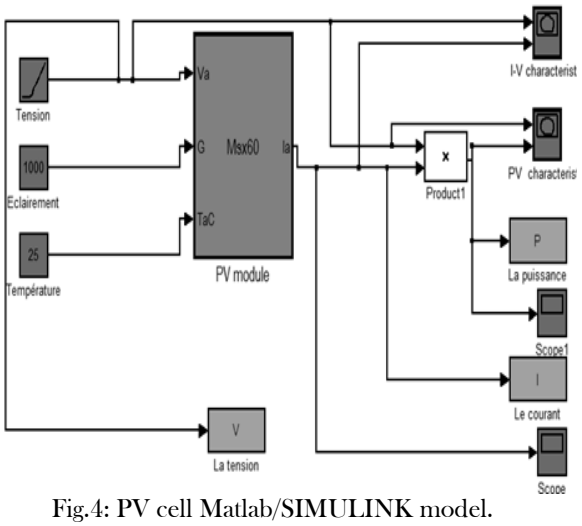
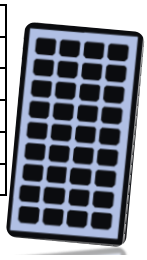


Fig.4: PV cell Matlab/SIMULINK model.

Table 3 Solarex MSX 60 PV Module specifications at 25 ° C [13].

Typical peak power (Pp)	60 W
Voltage at peak power (Vpp)	17.1 V
Current at peak power (Ipp)	3.5 A
Short-circuit current (ISC)	3.8 A
Open-circuit voltage (Voc)	21.1 V
Number of series cells	36



The shape of the current-voltage characteristics I(V) and frequency power P (V) obtained using the electric model equations presented in Figure (5) and figure (6).

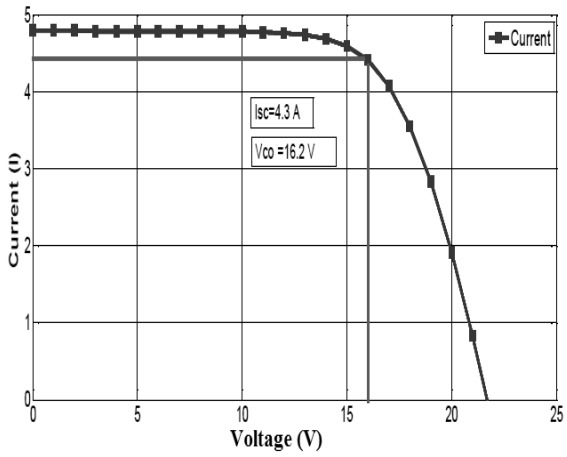


Fig.5: Current-voltage characteristics of the PV cell

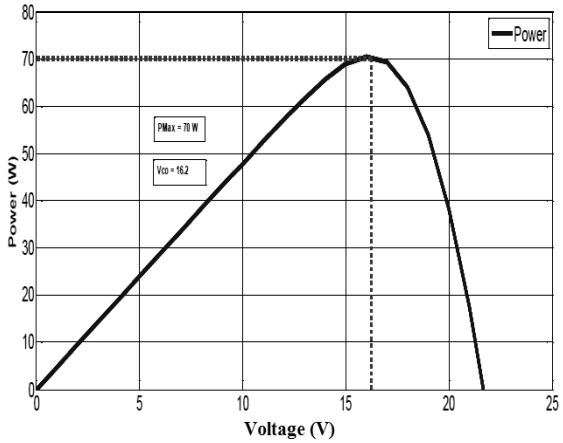


Fig.6: Power-voltage characteristics of the PV cell

5. Influence of the internal and external parameters of the characteristic (Ipv -Vp) of a photovoltaic cell

5.1. External parameters

5.1.1. Effect of radiation

The increase of the illumination with a temperature fixed causes an increase or generator operates as a current generator, but it is one of the increase in the voltage to égerment open circuit, the current is directly proportional to sunlight where the short-circuit current (Isc) is clearly sensitive to sunlight, For against the voltage is relatively un degraded. We deduce so that the cell can provide a voltage near that correct, even in low lighting.

Finally, when the sun raises, the intensity of short circuit increases, the curves characteristics shift to values growing, allowing the module to produce an largest electric power.

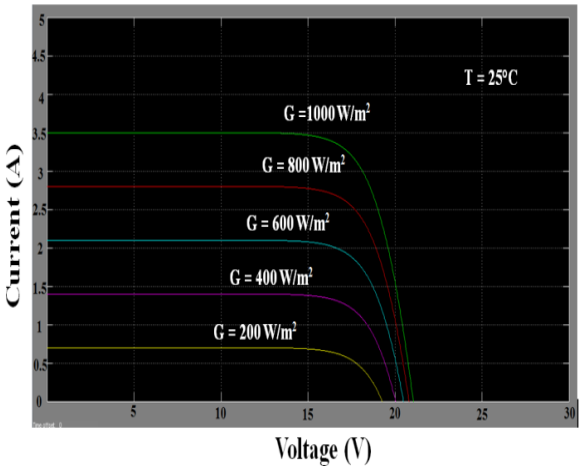


Fig.7: Current-voltage Characteristics for different irradiationat T = 25 ° C.

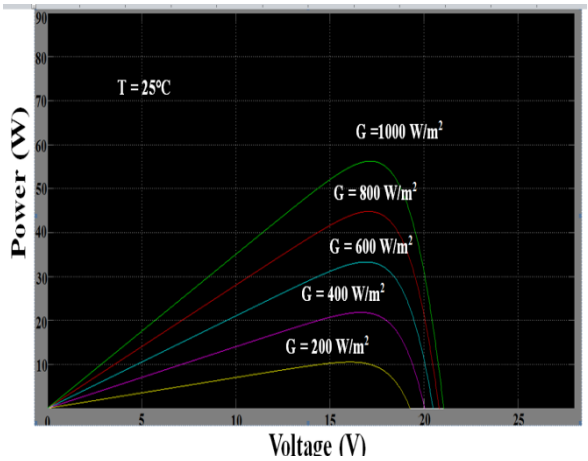


Fig.8: Power-voltage Characteristics for different irradiation at T = 25 ° C.

5.1.2. Influence of temperature

Temperature is an important parameter in the cell behavior. Increasing temperature with a fixed illumination causes net reduction of the open circuit voltage (Voc) and an increase in the short-circuit current (Isc), and a reduction of the maximum power (Pmax). The influence of temperature is reduced compared to the sun, but it is not negligible on the current / voltage characteristic of a generator. To a temperature which changes from 0 to 100 ° C, it can be seen that the variation of the voltage changes much more than the current. It varies very slightly. Unlike voltage, short-circuit current, meanwhile, increases with an increase in temperature.

This is due to better absorption of light, the optical gap with lowering the increase. However, this increase in intensity is very low; it can be neglected to the point of maximum power.

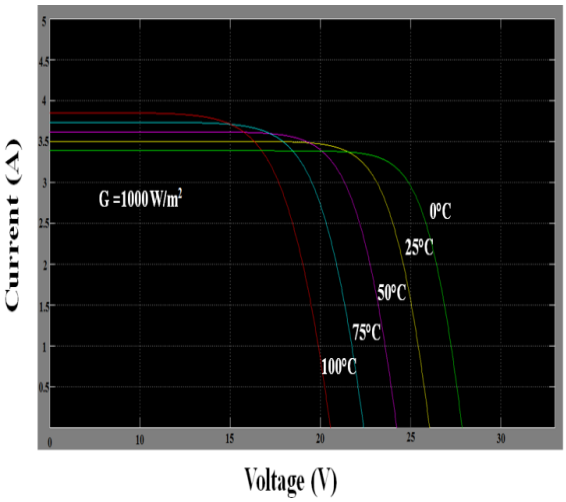


Fig.9: Current-voltage Characteristics for different temperature at G= 1000 W /m².

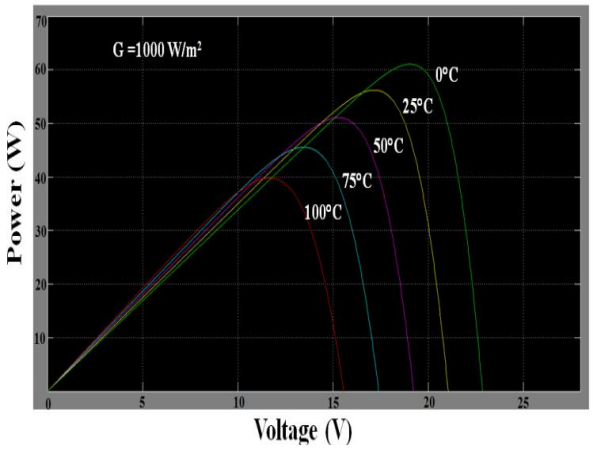


Fig.10: Power-voltage Characteristics for different temperature at G= 1000 W /m².

5.2. Internal parameters

5.2.1. Influence of series resistance

The series resistance is the slope of the characteristic in the area where the photodiode acts as a voltage generator, and when it is high, it decreases the short circuit current value (Icc).

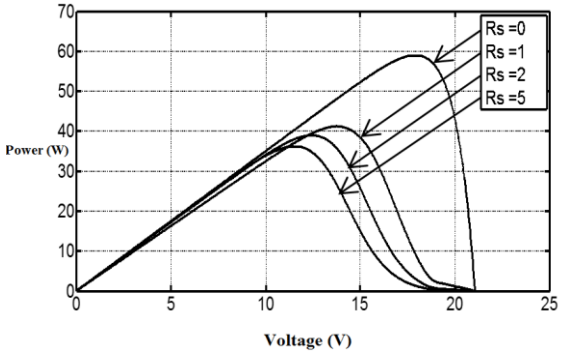


Fig.11 Influence of series resistance on P (V)

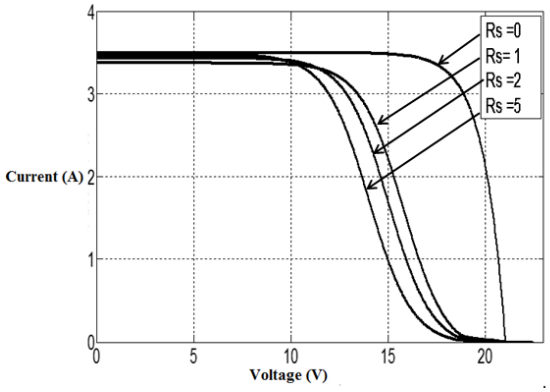


Fig.12: series resistance Influence on I (V)

5.2.2. Influence of the quality factor

The increase of the diode ideality factor inversely affects the area or point of maximum power and this is reflected by a decrease power level of the area of operation. [18]

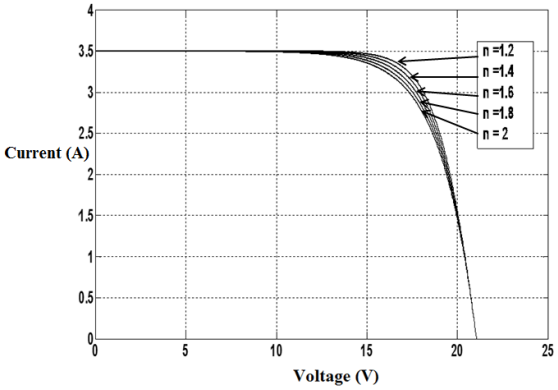


Fig.13: Quality factor influence on I (V)

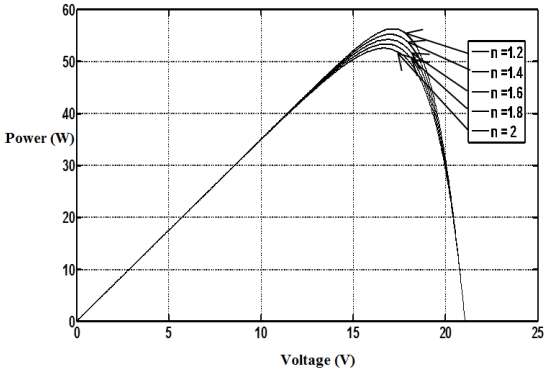


Fig.14: Quality factor influence on P (V)

5.2.3. Influence of saturation current Is

Figures (15 and 16) below illustrate the effect of saturation current Is on the characteristic I(V) and P(V) of the solar cell under illumination; It is found that increasing the saturation current (Is) for the diode causes a reduction of the open circuit voltage

(VCO) by against the short-circuit current (Isc) remains constant.

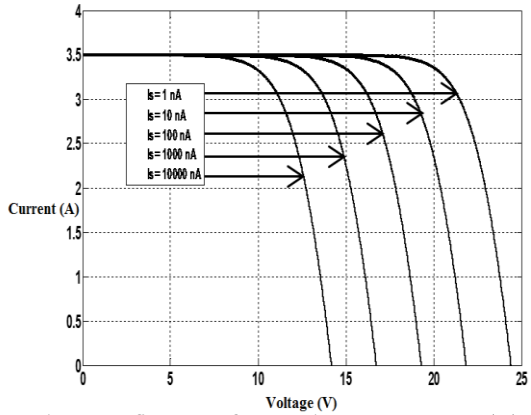


Fig.15: Influence of saturation current on I (V)

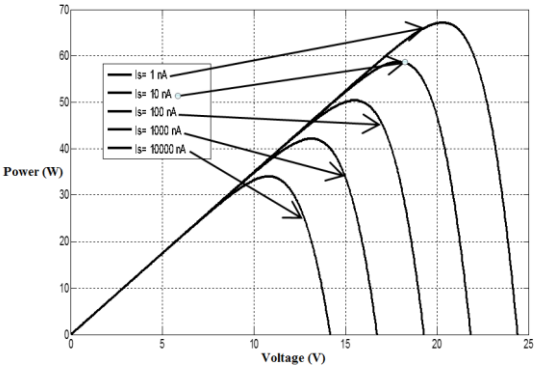


Fig.16: Influence of saturation current on P (V)

5.2.4. Influence of the shunt conductance (parallel)

Figures (17 and 18) below illustrate the effect of the resistance Rp parallel on the I(V) and P(V) characteristic of the cell under solar illumination. Note that the voltage open circuit (Vco) and the short-circuit current (Isc) does are not changed; but the characteristic deforms very quickly, this influence is reflected in increase in the slope of the I(V) characteristic of the cell in the area corresponding to an operation as a power source (low voltage).

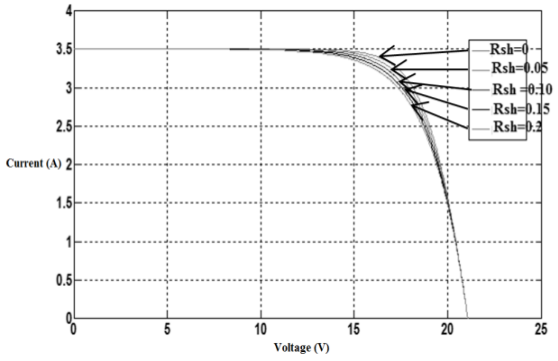


Fig.17 Influence of quality of the shunt resistance on I (V)

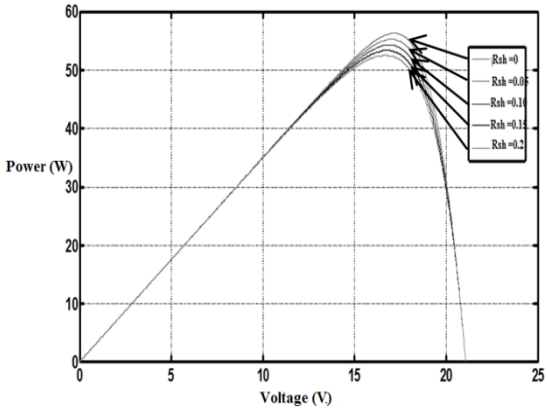


Fig.18 Influence of quality of the shunt resistance on P (V)

6. Conclusion

In this article, we presented the various simulations of the electrical characteristics of the model electrical equivalent of the photovoltaic cell, we can note that the power output of a solar panel does not depend only on the radiation and temperature of the exposure, but also parameters internal (series resistance, shunt resistance, idealityfactor, and the saturation current).

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