A Simplified Diagnosis Method for CHBMIs under Open-circuit Switch or Battery Faults

Omar Kherif, Tahar Zebbadji, Youcef Gherbi, Mohamed Larbi Azzouze, and Madjid Teguar

Abstract—This paper deals with the diagnosis of cascaded H-bridge multilevel inverters controlled by a sinusoidal level-shifted pulse-width modulation technique. For this purpose, the behaviour of 3, 5, 7 and 9-level inverters is studied for regular and faulty operation modes. Three types of recurring faults are considered, namely open-circuit of a switch, damaged and disconnected battery. Under a single fault, the output voltage signals are presented where the impact of each fault is discussed. In order to detect, identify and localise the three types of fault, a signal processing method is proposed, elaborating the output voltage of inverters with and without fault. The obtained results are convincing for the considered cases. The study shows no real correlation between the selected features from one to the other type of fault. Indeed, each fault type has its own trajectory with respect to the evolution of the output voltage characteristics. Thus, localizing the faulty component within the multilevel inverter can be made with no ambiguity. Such findings obviously solve a large part of problems associated with the presence of faults in multilevel inverters. They can help improving the reliability of the inverter in such way it continues working.

***Keywords*—Cascaded H-Bridge, Diagnosis, Multilevel inverter, Industrial electronics, Voltage source inverter.**

I. Introduction

Multilevel inverters represent an ideal choice of the high-power demands for electric drives and renewable energies exploitation. These inverters might be considered as an important alternative in the area of high-power medium-voltage energy control with almost a high-quality output with low harmonic distortion [1]. Among many inverter's topologies, cascaded H-bridge multilevel inverter (CHBMI) presents an easier topology to implement with practically reduced harmonics [2]. CHBMIs are typically used to eliminate the bulky transformer required in the case of conventional multiphase inverters. These inverter also used to eliminate the clamping diodes and the flying capacitors required, respectively, in the case of diode and flying capacitor inverters [3, 4]. However, these, on one hand, require a large number of isolated voltage sources to supply each cell and, on the other hand, the number of switches needed increases accordingly. Thus, the fault probability of the accompanying system raises [5, 6].

The reliability of CHBMI has received much attention from researchers due to the occurrence of various faults within the system (e.g., [7–10]). An unbalanced voltage is generated when a fault occurs which can produce permanent damage to the load or complete system failure [8]. Most of these faults occur in switching devices, circuit boards, capacitors, and power sources [11]. If these faults are not fixed, a considerable negative impact on the performance of the inverter and the system to which it is connected will be observed [11]. The thermal factor might be considered as a source of disturbance that has more impact on the reliability of power electronics components and systems with a rate of 55%. Indeed, other factors such as humidity and vibrations are very often linked to the degradation of power devices [12].

In fact, CHBMI are currently utilized in an enormous variety of industrial applications, including variable speed AC drives. However, these inverters are quite susceptible to switch failures due to their complexity and exposure to several stresses [5]. According to [12], semiconductor defects account for 34% of failures in converter systems. Based on more than 200 products from 80 companies, semiconductor power devices were selected by 31% of respondents as being the most fragile components [12]. Capacitor faults include open-circuit/short-circuit, displacement of materials between electrodes creating a conductive path, dielectric breakdown, etc. [13]. In addition, PCB defects include broken metal pipes, corrosion or cracking of traces, misalignment of components, delamination of boards and cold welds [13].

Choi et *al.* [12] analysed the different methods of study and treatment of switch failures, giving statistics on this aspect. According to [8], on one hand, the short-circuit fault is difficult to handle because an abnormal over-current which can cause serious damage to other parts is produced immediately. On the other hand, the open-switch fault increases total harmonic distortion and adversely affects the grid, which is connected to. In literature, there is a great interest in detecting the faults that could occur in the controllable devices of multilevel inverters (e.g., [6, 14–16]). In [6] and [14], the detection method used a wavelet packet transform and a neural network algorithm without additional devices. Also, the current pattern by the

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open-switch fault of the two-level topology was used, in which, the detection method has been carried out using a differential equation of currents [15]. Therefore, most of the diagnostic methods for open-circuit faults have been practically focused on the occurrence of single faults. In addition, other works have the capability to handle and identify multiple failures (e.g., [10]). The average absolute values have been used here as prime quantities to formulate the diagnostic variables.

Indeed, any failure at a given level of the multi-level converter can cause abnormal operation of the electrical system. In electric drives, such a failure can cause the motor to overheat, increasing harmonics and acoustic noises, etc. Sometimes the need to shut down the entire drive system arises to avoid serious damage. To reduce downtime and therefore improve productivity, it is necessary to detect faults in converters in order to fix them [17]. It is well known that diagnosing faults in multilevel inverters is a difficult task requiring efficient and rapid decision-making procedures especially under extreme noisy measurement conditions, strongly interdependent data, large number of inputs and a complex interaction between symptoms and faults [1]. The diagnosis consists in locating the fault, and this, by comparing the current state of the system according to the readings of the sensors compared to that of normal operation [18]. Better understanding of the system dynamics might be a key factor that leads to a successful application, decreasing losses and improving the quality of the output voltage waveforms.

In this paper, simulation tests have been carried out to study a CHBMI under different possible faults. One switching device within the inverter has been affected by open-circuit faults. Also, the malfunction or disconnection of one DC link has been considered. Based on the output voltage records, the effects of the selected faults have been examined and the output voltage has been presented accordingly. The obtained results show the possibility to visually distinguish the fault features compared with the regular operation mode. Using the output voltages, THD, a_0, A_f, RMSE and STD have been used to extract information corresponding to the fault detection, identification and localisation. The obtained results confirm the effectiveness of the proposed fault diagnostic approach for 3, 5, 7, and 9-level inverters. Diagnostic results and the information on the identified faulty switches and batteries in multilevel converters can help to reduce the downtime cost of industrial power electronic systems.

II. Inverter Topology and Control Strategy

A. CHBMI Topology

Fig. 1 shows the circuit configuration of the selected three-phases power-conversion multilevel inverter.

The circuit has N-number of H-Bridge per phase, providing approximately a sinusoidal output voltage. For each phase, this later is the sum of the voltages that are generated by each cell. A given H-Bridge has been made up of four switches namely S_{1i}, S_{3i}, S_{2i} and S_{4i}, having an independent DC voltage source $V_{in} = E = E_i$.

The output voltage phase is synthesized by the sum of inverter outputs. Each single-phase full bridge inverter can generate three level outputs, $+E$, 0, and $-E$. This is made possible

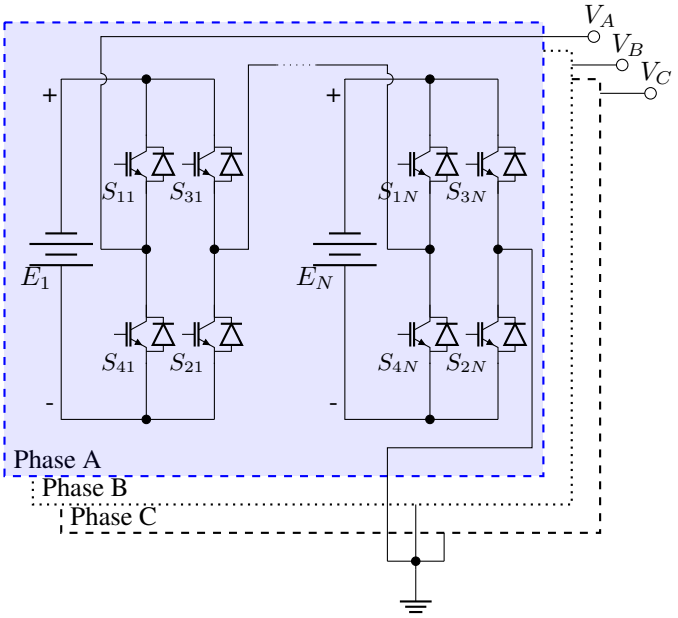
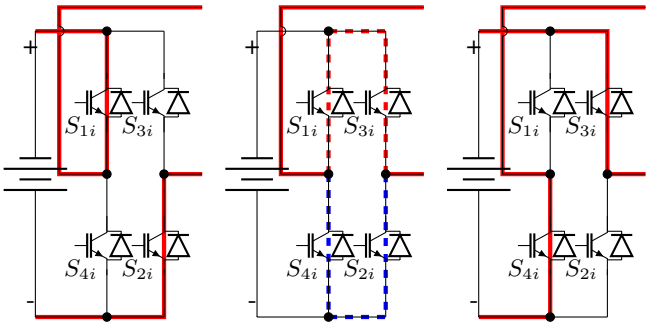


Fig. 1: Circuit configuration of the three-phase CHBMI

by connecting the DC sources sequentially to the AC side via the four semiconductor power devices. Fig. 2 illustrates the voltage polarities according to the switching states for each H-bridge(positive, zero and negative polarities in Figs. 2(a), 2(b) and 2(c), respectively).



(a) Positive polarity (b) Zero polarity (c) Negative polarity

Fig. 2: Output voltage polarities for each H-bridge

From Fig. 2, a positive polarity is obtained for the case where S_{1i} is activated and S_{3i} is deactivated. The negative polarity appears for the complementary case. Moreover, the zero polarity is obtained during the simultaneous activation or deactivation of the switches (S_{1i} and S_{3i}). Table I summarizes the switching states of the 3-level inverter (only one H bridge). It is worth noting that the state of switch is designted by 1 or 0 when it is on ON-state or OFF-state, respectively.

For 5, 7 and 9-level inverter, a second, third and fourth block (bridge H) are added in cascade per phase, respectively. Each inverter will have the same three voltage levels, namely $+E$, 0 and $-E$ for every cycle. By cascading the output voltage of the H-bridge inverters per phase, a stepped voltage waveform is produced. It is well known that the level number of the output voltage is defined by $m = 2s + 1$, in which s is the number of DC sources or the cascaded H-bridges per leg. It is worth noting that the three output voltages of the three-phase cascaded

Table. I
SWITCHING STATES OF A H-BRIDGE INVERTER

Output voltage	Switching states	
V_A	S_{1i}	S_{3i}
E	1	0
0	1	1
0	0	0
-E	0	1

inverters can be connected in either wye or delta connection. The line voltage is equal to the phase voltage in delta connection. However, the line voltage is obtained by subtracting two phase voltages in wye connection. In this topology, the maximum number of levels is $m = 4s + 1$ and triplen harmonics are eliminated.

B. Control and Modulation Strategy

Multi-carrier PWM method is embraced in this investigation to achieve an approximately sinusoidal output voltage waveform per phase. In this method, PWM signals are generated by comparing a reference signal of sinusoidal form with triangular carriers. Three sinusoidal signals, shifted by $(2\pi/3)$–angle, are required for the three output voltages. Recall that for an inverter of N levels, there must be $(N-1)$ triangular carriers with the same frequency and amplitude, constituting the level shifted PWM (LS-PWM). Fig. 3 shows an example of the control signals for generating the pulses of the switches of a 5-level CHBMI, in which a switching frequency $F_c = 1kHz$ has been selected with a modulation ratio $M_i = 1$.

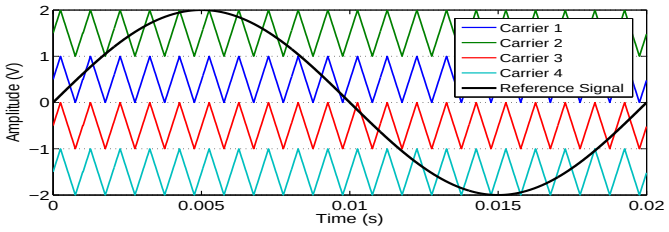


Fig. 3: PWM strategy for the 5-level CHBMI

Phase disposition strategy is used for the carrier arrangements (i.e., in phase with each other), which have the same peak to peak amplitude and F_c frequency. In this modulation technique, the sinusoidal reference is constantly compared with each of the triangular signals. If the reference is greater than the triangular signal, the switch corresponding to this modulation is active. Otherwise, the switch in question is in the ON state. For each sine signal, four features are obtained with respect to the four carriers. Fig. 4 illustrates an example of the triggering pulses obtained for the 5-level CHBMI.

III. FAULTY OPERATION MODE RESULTS

In this section, regular and faulty operation modes of the three-phase 3, 5, 7 and 9-level CHBMI have been presented. Each inverter has been simulated in MATLAB environment to assess the proposed fault detection technique. DC voltage sources of $30V$ have been considered with a fundamental frequency (f) of 50Hz and sampling (f_s) of 5kHz.

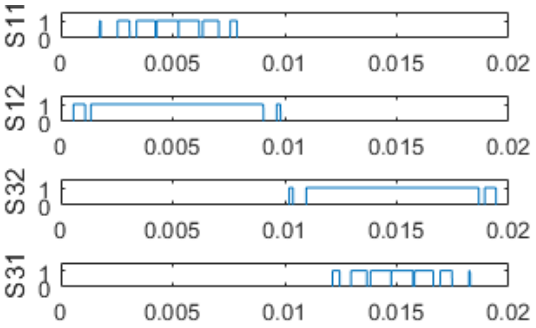


Fig. 4: Triggering pulses for the 5-level CHBMI

A. Open-Circuit Fault (Type I)

In this part, simulations have been carried out to show the effect of switches' open-circuit faults on the inverter output voltages. Fig. 5 shows the output voltage patterns, recorded for fault of one selected switch in the considered inverter. Figs. 5(a), 5(b), 5(c) and 5(d) show the effect of open–fault in CHBMI of 3, 5, 7, and 9 levels, respectively.

For regular operation mode (Fig. 5), each output voltage can be represented by Fourier series, in which the waveform is given as follows:

$$V(t) = \sum_{n=1}^{\infty} V_n \sin(n\omega t), \qquad \omega = 2\pi f \tag{1}$$

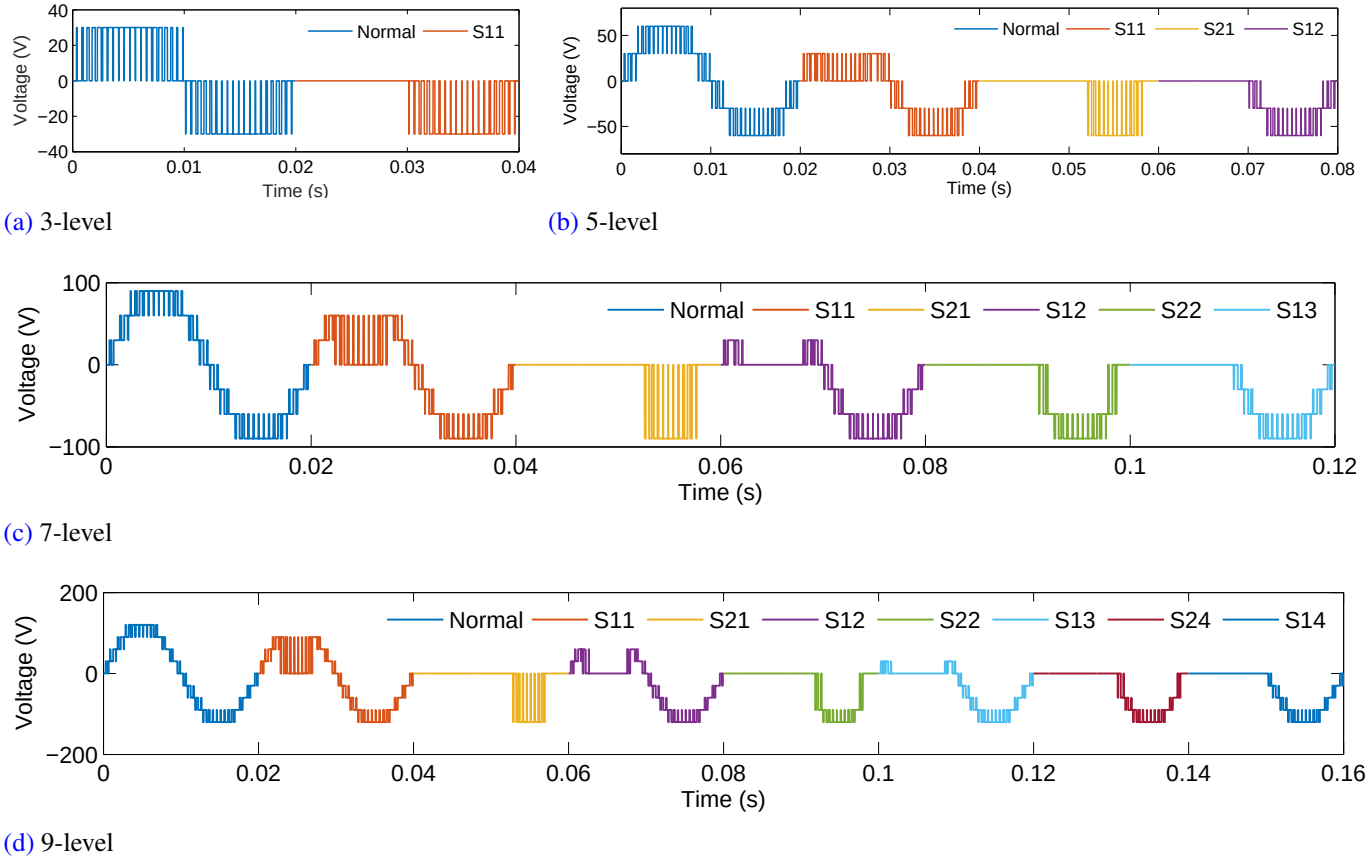
where, V_n is the amplitude of n-th voltage harmonic that is given by:

$$V_n = \begin{cases} \frac{4}{n\pi} \sum_{k=1}^{s} V_{dc} \cos(n\alpha_k) & \text{for odd n} \\ 0 & \text{for even n} \end{cases} \tag{2}$$

in which, s is the number of H-bridges and α_k is the switching angle used in the study $(2\pi/3)$.

Compared to the regular operation mode, one can see that all fault features in open-circuit cases could be visually detected. Fault in a particular switch within a given leg leads to a deformation on the output voltage of the corresponding phase related to this leg. For a single H-bridge, the failure of a switch causes the disappearance of the positive or negative part of the output voltage. The distorted output signal due to the open circuit type fault of switch S_{11} is exactly the same as that of S_{21} where only the negative part of the signal appeared. Regarding a fault at switch S_{31} or S_{41} (they have the same waveform), the output voltage contains only the positive part of the signal associated with regular operation. Therefore, only one spectrum can be found, describing the open circuit fault in a 3-level inverter as shown in Fig. 5(a)

Referring to the results of Fig. 5(b), three types of deformations have been noticed at the level of the output signal: two waveforms for a fault in H_1 and another waveform for H_2. The first one consist in the absence of $\pm 2E$ $(\pm 60V)$ levels in some intervals. For the second voltage waveform, there is a disappearance of $\pm E$ $(\pm 30V)$ levels with zero voltage levels during a time interval greater than half period. The complete absence of either positive or negative sequences is characterising the third waveform. Indeed, a type I fault of S_{11} and S_{31} brings out the same



(a) 3-level (b) 5-level

(c) 7-level

(d) 9-level

Fig. 5: Output voltage of the 3, 5, 7 and 9-level inverters during a type I fault and normal operation mode

waveform with symmetrical characteristics with respect to the time axis. The same observation is perceived for the following pairs of switches: (S_{41} and S_{21}), (S_{12} and S_{32}) and (S_{22} and S_{42}). It should be noted that the waveform obtained for a type I fault of S_{12} and S_{22} are identical. Thus, if we consider the spectrum of the output voltage signal, three waveforms can be identified: the first waveform concerns the switches S_{11} and S_{31}, the second one is related to those of S_{21} and S_{41} and the last one is linked to those of S_{12}, S_{22}, S_{32}, and S_{42}.

From the results of Figs. 5(c) and 5(d), one can generalize the study to an N-level inverter system according to the output signals associated to a type I fault of a given switch. In this condition, a number $(N-2)$ of signal waveforms is obtained for an N-level inverter. Thereafter, the waveforms for each H-bridge are briefly described as follows:

1. Type I fault on H_1 :
   - In the switch S_{11} (S_{31} respectively): The deformation consists in the disappearance of the last level $(N-1)E/2$ in the positive (negative respectively) cap. In addition, during the interval where S_{11} (S_{31} respectively) is active, the voltage levels vary from 0 to $((N-1)/2-1)E$ in the positive (negative respectively) cap.
   - In the switch S_{41} (S_{21} respectively): The output voltage is zero except for the operating interval of S_{11} (S_{31} respectively) where it varies directly between 0 and $(N-1)E/2$.
2. Type I fault on H_i :
   - In the switch S_{1i} (S_{3i} respectively): The voltage is null during the ON-state interval of S_{1i} (S_{3i} respectively).
   - In the switch S_{4i} (S_{2i} respectively): The voltage is null during the whole period except the ON-state interval of S_{1i} (S_{3i} respectively).
3. Type I fault on H_N : The distorted output voltage following the appearance of a fault in S_{1n} is exactly the same as that in S_{2n}. The same observation is obtained for the two other switches (S_{3n} and S_{4n}). These two signals are also symmetrical with respect to the time axis with a phase shift of π.

B. Battery Fault Type II

Under particular conditions such as the batteries ageing, a DC source might be lost. The effect of such a fault has been investigated in this part where the internal resistor has been neglected. Fig. 6 shows the output voltages of the 9-level inverter such that the bridges H_1, H_2, H_3 and H_4 are in sequence way one after one under the type II fault.

In this figure, the obtained four signals can be overlapped to clarify the difference between the defected batteries. A common result between these four signals is the loss of the last level of voltage $(N-1)E/2$ ($4E$ in this case). It is true that there are 3 levels of voltage left, however, the arrangement of the remaining

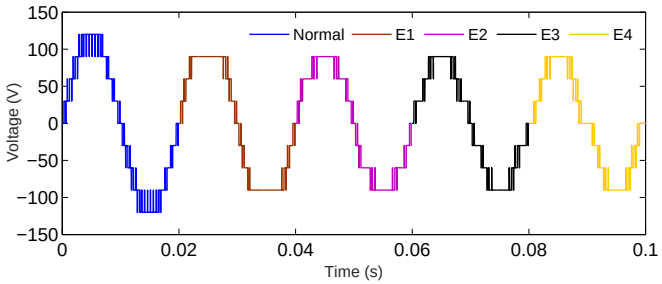


Fig. 6: Output voltages under type II fault in the CHBMI

levels is different. One can notice that a type II fault on the H_1 bridge, the 120V level is replaced by the one of 90V. A type II fault affecting the H_2 bridge generates the same waveform of signal found previously but with a slight decrease in the duration of the $90V$ level. For the fault concerning the H_3 bridge, we note that the duration of the $60V$ level has decreased slightly compared to that of the fault of the H_2 bridge. Whereas, for the fault concerning bridge H_4, the duration of the $30V$ level has decreased compared to that of the fault of bridge H_3. This means that the duration of each level is directly linked to the fault affecting a given bridge (H_i). This duration can be quantified by the control sequences of the different switches of a given bridge (see Fig. 6).

C. Battery Fault Type III

In this part, the battery of a given bridge is totally disconnected, hence, open-circuit at the input side of this bridge is obtained. Fig. 7 shows the V_{AN} output voltages of the 9-level inverter respectively for a fault in the battery disconnection of H_1, H_2, H_3 and H_4.

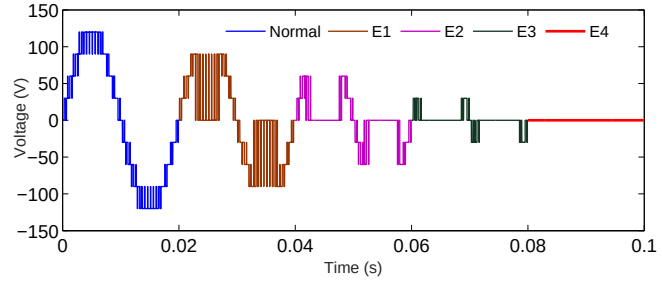


Fig. 7: Output voltages under type III fault in the CHBMI

Each battery contributes in a different way depending on its order of connection within the multilevel inverter. This means that the time contribution for each level is different from the other (see Fig. 7). Disconnecting a battery from a given bridge completely opens the phase for a well-defined period. By disconnecting the battery from the H_1 and for a modulation index equal to the unit, we notice the same phenomenon as that obtained for a simultaneous type I fault of S_{11} and S_{31}. Likewise, a type III fault affecting the H_i bridge is equivalent to a simultaneous type I fault of the switches S_{1i} and S_{3i}. By disconnecting the battery from the H_n bridges, one can notice that during the application of its own voltage E, the output voltage (V_{AN}) is null. It can be noted that the application duration of the voltage E associated to H_4 is observed throughout the period. Therefore, the voltage V_{AN} is null for the entire duration of the type III fault.

IV. Fault Diagnosis Method

A. Features Extraction Technique

In this section, a signal processing technique is presented, allowing the analysis of electrical signals in order to extract information useful for the detection and characterization of type faults (I, II and III). This method is based on the frequency decomposition of the signals, and this allows computing the THD, the mean value, the standard deviation and the root mean square error of the signals to be analysed in MATLAB environment. The frequency spectrum of a signal has been computed with and without faulty operation. Thereafter, the different parameters have been calculated.

Fourier series decomposition helps with the computation of the signal THD and the fundamental amplitude, which describe the quality of the output waveform. The signal mean value of the output voltage is the average of the instantaneous values measured over a full period, corresponding to the first component of the signal FFT. In addition, the standard deviation indicates the degree of variation or dispersion compared to the average (average or expected value). A low standard deviation indicates that the data points tend to be very close to the mean, while a high standard deviation indicates that the data is spread over a wide range of values.

B. Features Extraction Results for Type I Fault

1— Type I Fault in 3-level CHBMI: For the 3-level inverter, Table II illustrates the computed values of the parameters used in this study. These parameters have been calculated with and without a faulty operation.

Table. II
FEATURES OF THE 3-LEVEL INVERTER UNDER TYPE I FAULT

Operation with/without type I fault	$\mathbf{V_{AN}}$				
	THD (%)	**A_f (V)**	**a_0 (%)**	**STD**	RMSE (%)
Without	52.36	29.99	0	23.93	0
S_{11} or S_{21}	85.87	14.99	−63.68	13.97	29.25
S_{31} or S_{41}	85.87	14.99	+63.68	13.97	29.25

From Table II, the results show remarkable differences between the values obtained during regular operation mode and that under fault. Indeed, the fault of one open-circuit switch generates a remarkable increase in THD from 52.36 % to 85.87 %, accompanied by a decrease in the amplitude of the fundamental (denoted A_f) from 29.99 V to 14.99 V. This is to say that this fault generates a strong voltage distortion. In addition, this anomaly causes an increase of the relative error of the output voltage signal, up to 29.25%. Moreover, a decrease in the standard deviation of the signal from 23.93 to 13.97 was recorded. In faultless operation of the inverter, the voltage signal is characterized by its null mean value. The type I fault generates a signal distortion for the S_{11} and S_{21} switches symmetrically compared to that of S_{41} and S_{31}, that is why the same mean output voltage value; having opposite signs, has been obtained.

From the disparities between the obtained results, it is concluded that the selected features are capable of detecting and locating the fault by indicating the opening of a switch on the same path,

i.e., S_{11} or S_{21} on one hand, or S_{31} or S_{41} on the other hand, without indicating the exact position of the open-circuit switch.

2— Type I Fault in 5-level CHBMI: In the case of 5-level inverter, Table III illustrates the different values of the features used during this investigation.

Table. III
FEATURES OF THE 5-LEVEL INVERTER UNDER TYPE I FAULT

Operation with/without type I fault	$\mathbf{V_{AN}}$				
	THD (%)	$\mathbf{A_f}$ (V)	$\mathbf{a_0}$ **(%)**	**STD**	RMSE **(%)**
Without	26.91	60.10	0	43.99	0
S_{11}	67.89	36.53	−35.93	31.22	23.01
S_{31}	67.89	36.53	+35.93	31.22	23.01
S_{21}	110.54	23.52	−55.73	24.79	36.26
S_{41}	110.54	23.52	+55.73	24.79	36.26
S_{12} or S_{22}	57.72	30.05	−63.68	24.52	24.52
S_{32} or S_{42}	57.72	30.05	+63.68	24.52	24.52

According to the results of Table III, the operating mode with an anomaly can be detected when the THD value is greater than 26.91%. The fault in this case can be classified into 3 groups, corresponding to the three waveforms of signals shown in Fig. 5(b). The first group represents a fault in the lower switches of H_1 (S_{41} and S_{21}) with a THD of 110.54%. The second group characterises a fault in the upper switches (S_{11} and S_{31}) of H_1 with a THD of 67.89%. Finally, the third group is related to an open-circuit fault in all switches of H_2, having a THD of 57.72%. Regarding the sign of the mean value (positive or negative), one can locate the faulty switch within the three given groups as follows:

- Group 1: positive value means that the fault is on S_{41}, otherwise S_{21}.
- Group 2: positive value means that the fault is on S_{31}, otherwise it is on S_{11}.
- Group 3: positive (respectively negative) value means that the fault is on S_{42} or S_{32} (respectively S_{12} or S_{22}).

In general, the followed approach allows locating the default position of the switch, with the exception of the last bridge (H_2) where it is possible to distinguish between the pairs of switches (S_{12} or S_{22}) and (S_{42} or S_{32}).

3— Type I Fault in 7-level CHBMI: Table IV summarizes the different values of the proposed features for the 7-level inverter with and without type I defect.

The difference in THD values allows identifying four groups of switches. The group 1, made up of the switches S_{41} and S_{21}, stands out with a THD of 130.51%. The signals whose THD is 62.63% (default on S_{11} and S_{31} with the upper switches of the bridge H_2) compose the group 2. For a fault in the lower switches of H_2, the THD is 69.84%. The group 4 concerns the fault of all the switches of H_3, which is characterised by a THD of 50.56%.

Table. IV
FEATURES OF THE 7-LEVEL INVERTER UNDER TYPE I FAULT

Operation with/without type I fault	$\mathbf{V_{AN}}$				
	THD (%)	$\mathbf{A_f}$ (V)	$\mathbf{a_0}$ **(%)**	**STD**	RMSE **(%)**
Without	18.26	89.92	0	64.63	0
S_{11}	60.94	60.48	−26.16	50.06	18.80
S_{31}	60.94	60.48	+26.16	50.06	18.80
S_{21}	130.51	29.50	−53.65	34.25	41.67
S_{41}	130.51	29.50	+53.65	34.25	41.67
S_{12}	62.63	47.31	−53.25	39.47	27.57
S_{32}	62.63	47.31	+53.25	39.47	27.57
S_{22}	69.84	42.63	−59.11	36.76	31.07
S_{42}	69.84	42,63	+59.11	36.76	31.07
S_{13} or S_{23}	50.56	44,95	−63.68	35.63	29.29
S_{33} or S_{43}	50.56	44.95	+63.68	35.63	29.29

At this point, one can use the other parameters such as the fundamental amplitude, the absolute value of the DC component, STD or RMSE to obtain two complementary subgroups (belong to the group 2). The first subgroup 2.1 is formed by the upper switches of H_1 (S_{11} and S_{31}) whose fundamental value is equal to 60.48V. The subgroup 2.2 contains the two switches of H_2 (S_{42} and S_{22}) with the fundamental value of around 40V. Moreover, to distinguish between the switches of each group/subgroup, the sign of the mean values has been elaborated as follows:

- Group 1: positive (respectively negative) value means that the fault is on S_{41} (respectively S_{21}).
- Subgroup 2.1: positive value means that the default is on S_{41}, otherwise S_{21}.
- Subgroup 2.2: positive value means that the default is on S_{32}, otherwise it is on S_{12}.
- Group 3: positive value means that the default is on the switch S_{42}, otherwise it is on S_{22}.
- Group 4: positive value indicates that the fault is on S_{43} or S_{33}, otherwise it is on S_{13} or S_{23}.

It is important to note that this approach requires more precision to distinguish between either the switches of subgroups 2.1 and 2.2 or the pairs (S_{13} or S_{23}) and (S_{33} or S_{43}) due to the fact that the parameters values are close to each other.

4— Type I Fault in 9-level CHBMI: Table V illustrates the different values of the parameters used for the 9-level inverter for the type I fault.

Based on the results of the computed THD, five groups of switches can be obtained as follows:

- Group 1 is associated to a fault on S_{41} and S_{21}, which has a THD of 145.22%.

Table. V
FEATURES OF THE 9-LEVEL INVERTER UNDER TYPE I FAULT

Operation with/without type I fault	$\mathbf{V_{AN}}$				
	THD (%)	$\mathbf{A_f}$ (V)	$\mathbf{a_0}$ **(%)**	**STD**	RMSE **(%)**
Without	13.83	120	0	85.64	0
S_{11}	56.61	85.47	-21.27	69.44	16.18
S_{31}	56.61	85.47	$+21.27$	69.44	16.18
S_{21}	145.22	34.51	-52.68	43.02	45.47
S_{41}	145.22	34.51	$+52.68$	43.02	45.47
S_{12}	64.52	66.91	-45.03	56.31	25.43
S_{32}	64.52	66.91	$+45.03$	56.31	25.43
S_{22}	81.75	53.07	-56.77	48.47	33.36
S_{42}	81.75	53.07	$+56.77$	48.47	33.36
S_{13}	56.08	61.23	-58.36	49.64	28.58
S_{33}	56.08	61.23	$+58.36$	49.64	28.58
S_{23}	58.51	58.75	-60.83	48.13	30.01
S_{43}	58.51	58.75	$+60.83$	48.13	30.01
S_{14} or S_{24}	47.65	59.99	-63.69	46.99	29.29
S_{34} or S_{44}	47.65	59.99	$+63.69$	46.99	29.29

- Group 2 represents an open-circuit fault of the upper switches of H_1 (S_{11} and S_{31}) and all those of H_3 where the THD is around 57%.
- Group 3 characterises faults in the upper switches of H_2 (S_{12} and S_{32}) with a THD equal to 64.52%.
- Group 4, having THD equal to 81.75%, is related to faults of the lower switches of H_2 (S_{42} and S_{22}).
- Group 5 is linked to open-circuit of the H_4 with a THD of 47.65%.

It is worth noting that each group contains at least 2 switches. To overcome the localisation problem, the maximum value of the fundamental, the absolute value of the DC component, STD and RMSE have been exploited. For instance, as with the 7-level inverter, the sign of the mean values (a_0) might be used as follows :

- Group 1: positive value of a_0 means that the fault is on S_{41}, otherwise it is on S_{21}.
- Group 2 : this group, containing 6 switches, has been subdivided into the following subgroups :
  - Subgroup 2.1: positive (respectively negative) value of 52.68V means that the fault is on S_{41} (respectively S_{21}).
  - Subgroup 2.2: positive (respectively negative) mean value of 58.36V concerns fault is on S_{33} (respectively S_{13}).
  - Subgroup 2.3: this subgroup is identified by mean value of 60.83V, which is related to a fault on S_{43} (respectively S_{23}) if its sign is positive (respectively negative).
- Group 3: positive value of a_0 means that the fault is on S_{32}, otherwise it is S_{12}.
- Group 4: positive (respectively negative) value of a_0 indicates that the fault is on S_{42} (respectively S_{22}).
- Group 5: positive value of a_0 means that the fault is on S_{43} or S_{34}, otherwise, it is on S_{14} or S_{24}.

C. Features Extraction Results for Type II Fault

The same aforementioned features have been taken into account to deal with the fault localisation of a faulty battery in a 9-level inverter. The extracted features have been computed and illustrated in Table VI.

Table. VI
FEATURES OF THE 9-LEVEL INVERTER UNDER TYPE II FAULT

Operation with/without type II fault	$\mathbf{V_{AN}}$				
	THD (%)	$\mathbf{A_f}$ (V)	$\mathbf{a_0}$ **(%)**	**STD**	RMSE **(%)**
Without	13.83	120	0	85.64	0
E_1	16.86	102.7	0	73.65	13.99
E_2	19.15	90.35	0	65.05	24.05
E_3	19.90	84.67	0	61.04	28.72
E_4	24.40	82.19	0	59.82	30.15

According to this table, one can observe that the mean value is null for all cases of this type of fault. This observation is due to the fact that the signals extracted after the appearance of a fault always remain symmetrical with respect to the time axis. This parameter no longer fits into the fault localisation. From the THD readings, the type II fault of battery E_1 and E_4 can be easily detected because their respective THD is 16.86% and 24.4% compared to the regular operation mode (THD=13.83%).

For the fault of battery E_2 and E_3, their THD values are practically close: 19.15 % and 19.90 %. To overcome this situation, the fundamental amplitude, STD and RMSE have been used. For type II fault of battery E_2 or E_3, these parameters are respectively equal to (90.35V, 65.05, 24.05%) and (84.67V, 61.04, 28.72%).

D. Features Extraction Results for Type III Fault

In this part, features have been extracted from the output voltage of the 9-level inverter under a type III fault. Table VII illustrates the different values of the selected parameters.

For this type of fault in a 9-level inverter, Table VII shows a remarkable difference in all features except for the mean value, which remains null. For the case of fault of the first three batteries (E_1, E_2, and E_3), one can note that the values of each parameter vary (increase or decrease) for a given feature compared to the regular operation mode. This is to say that such a fault is easily detected. For the localisation purpose, the THD and RMSE increase from fault in the battery E_1 to E_3. The intermediate values of THD and RMSE allow concluding that the battery E_2 is defected. In addition, fault in the battery E_1 is identified by a higher value of the fundamental amplitude (50.96V), which decreases to 13.85V and 2.49V for a fault in the

Table. VII
FEATURES OF THE 9-LEVEL INVERTER UNDER TYPE III FAULT

Operation with and without type III fault	$\mathbf{V_{AN}}$				
	THD (%)	**A_f** (V)	**a_0 (%)**	**STD**	RMSE (%)
Without	13.83	120	0	85.64	0
E_1	113.52	50.96	0	54.51	36.35
E_2	274.96	13.85	0	28,66	66.54
E_3	684.09	2.49	0	12.17	85.79
E_4	–	0	0	0	100

battery E_2 and E_3, respectively. For the case of the last battery (E_4), almost all the parameters are null for the output voltage with the exception of RMSE (100%) and the THD. Therefore, for a right diagnosis, it would be wise to take into account the phase-to-phase voltage.

E. Features Extraction Comparison

From the obtained results of the proposed diagnostic method, it is possible to distinguish between regular operation mode (without fault) and that in the presence of a type I, II or III fault. This distinction is ensured by the use of the vector [THD, A_f, a_0, STD, RMSE]. One can recall that obtaining a non-null mean value, a_0, of the voltage signal, means that a type I fault is faced. However, a null mean value, of this, implies a type II or III fault. Parameters, other than the average value, make possible distinguish between these last two types of fault. In addition to the mean value a_0, two parameters (THD and A_f) are largely sufficient, in the actual case, to separate between the different types or at least between those of II and III, as illustrated in Fig. 8.

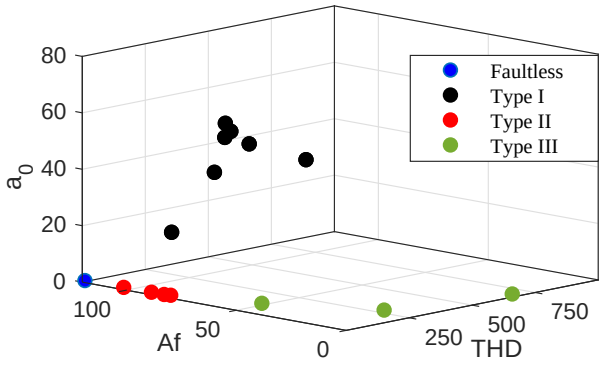


Fig. 8: Parameters distribution with respect to the type of faults for 9-level inverter

Regular operation is indicated by the blue dot. Likewise, the three assemblies presenting the three types of faults are isolated from each other. Since the features round up in separated groups in Fig. 8, the proposed method confirms the absence of correlation between the different types of faults considered. In general, the more uncorrelated the features, the better the classifier performance, which improves the identification process.

V. CONCLUSION

This paper dealt with the diagnosis of CHBMI under typical faults where their effects have been examined. First, fault in one of the controllable components has been considered, in which an open-fault case has been selected (Type I). Then, DC link faults have been studied for defected (Type II) and disconnected (Type III) battery. Simulations show the possibility to visually distinguish the fault features from the output voltage signal compared to the regular one. Based on the obtained results, a diagnostic method has been proposed using THD, A_f (amplitude of the fundamental), a_0 (mean value), STD (standard deviation) and RMSE (the mean square error) of the output voltage signal. The first three parameters are largely sufficient to distinguish between the three types of faults. This is due to the total lack of correlation between these faults. The location of faults is done by a classification according to their THD. Faults in switches with the same THD order have been classified in the same group. The other parameters allow further decision between the groups formerly considered. The three types of faults can be identified since the selected features are round up in separated groups. Such findings and the proposed technique might be used to extract a general fault diagnosis method to detect and locate the fault in higher level CHBMIs. The diagnostic results and the information on the identified faulty switches in multilevel converters can help the reduction of the downtime cost of industrial power electronic systems.

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