ANALYSIS OF GENERATION CURRENT IN AMORPHOUS SILICON THIN FILM TRANSISTORS
STUDY OF FILM THICKNESS EFFECT

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Abstract

Recently, there has been a growing interest in polysilicon thin film transistors (TFT's) . The purpose of this work is to study the effect of film thickness on the generation current. This study consists of an analysis of experimental transfer characteristics for different active layer thicknesses and a calculation of the generation current, starting from these curves in order to explain its variation as a function of gate voltage, for all the range of studied thicknesses, based on solving Poisson's equation. The results show that this current is field assisted, and that the position of parallel grain boundary plays a fundamental role in the behavior of this current as a function of film thickness.

Résumé

Le silicium polycristallin connaît de plus en plus un grand intérêt dans la fabrication des transistors en couches minces. Le but de ce travail est l'étude du courant de génération observé en mode de déplétion en fonction de l'épaisseur du film. Cette étude consiste en une analyse des caractéristiques de transfert expérimentales, de calculer et d'expliquer par la suite la variation du courant de génération dans toute la gamme des épaisseurs étudiées, en se basant sur la résolution numérique de l'équation de Poisson. Les résultats montrent que ce courant est assisté par champ et que la position du joint de grain parallèle joue un rôle fondamental dans l'évolution de celui-ci en fonction de l'épaisseur du film polycristallin.

Keywords : Polysilicon, Poole-Frenkel Effect, electrostatic coupling

1-Introduction

Amorphous –silicon device technology has played a dominant role in large area electronics. In this paper, we have developed a numerical method to explain the evolution of generation current versus gate voltage. In our simulation, the amorphous-silicon layer is modelised by a series of monocrystalline silicon crystallites separated by identical grains boundaries, parallel and perpendicular to the Sio_2/polycrystalline interfaces. Our computer model is based on the solving of a two-dimension Poisson's equation which inform us about the electric field, responsible of the amplification of the current in depletion mode, in relation with the granular structure of the active layer such as grain sizes, and intergranular traps density. The numerical simulation allows us to study the variation of the generation current versus layer thickness. We first describe the physical model used in this study. Next, we present our simulated results which are discussed.

2-The studied structure

Fig 1 shows a schematic cross section of the MOSFET. The starting material for device fabrication was silicon wafers. A 100nm SiO2 layer was thermally grown on RCA cleaned substrates. The polysilicon thin films were deposited using low pressure chemical vapor deposition (LPVCD) technique. Channel doping was carried out by ion implantation of boron with dose of 6e12cm^{-2} (1e17cm^{-3}). Source and drain were formed by 3e20cm^{-3} boron implantation, and are assumed to extend in the whole thickness of polycrystalline layer. The gate oxide was grown to a thickness of 100nm. At the end, contact regions were opened for AL metallization.

Observation under sweep electron microscope requires a very high resolution. It can inform us about layer's structure: disposition and grain side sizes. After a transverse cross section of the transistor, and a chemical attack of polysilicon by reagents, the examination shows that the amorphous –silicon layers are composed of two layers of grains, with comparable grain sizes, relatively large (L_L: 150 –250 nm). In contact with the substrate, there is a thin disturbed layer fig (2).

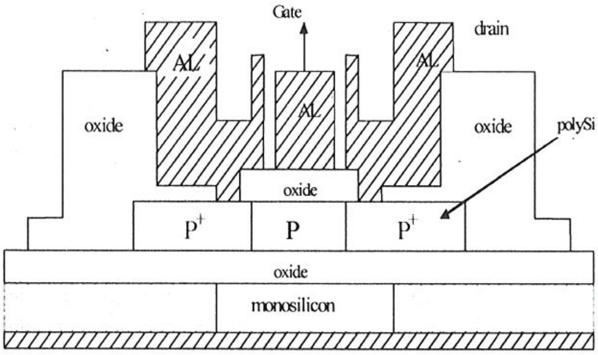

Fig1 :Polycrystalline silicon thin film transistor structure used in the study

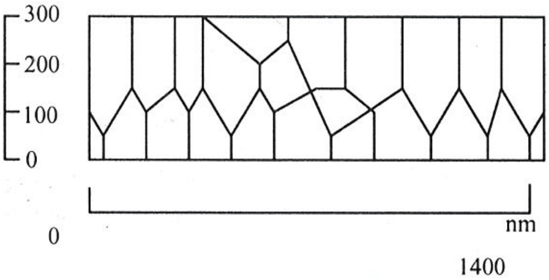

Fig 2 : structure of amorphous silicon films

3- Analysis of the generation current

In order to study the generation current versus different film thicknesses, reactive ion etching (RIE) process is implemented. Thus, after doping and annealing of the polycrystalline layer, the etching of polysilicon is carried out in the ionization chamber, using a plasma of SF_6. This operation is systematically followed of RCA cleaning to restore partially or completely the original quality of surface.

In depletion regime, the behavior of the studied structure is characterized by the leakage current I_L, constituted by the sum of two components with different origins: the residual current coming from ohmic conduction of polycrystalline layer between source and drain contacts, and the generation current which is field assisted[1].Thus, from the experimental transfer characteristics $I_{DS}=f(V_{GS})$ plotted in "off state", we can calculate the generation current. It is defined as the difference between the leakage current I_L, and the residual current I_R obtained when the structure is in a flat band regime[1]. Fig (3) shows the generation current versus active layer thickness, for different gate voltages.

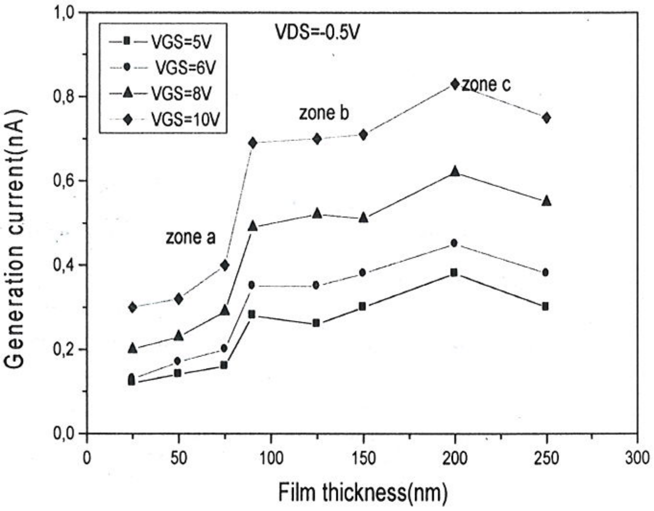

Fig 3: generation current versus film thickness for various gate voltages

3.1-Variation of the generation current (I_G) as a function of film thickness (t_f)

We notice that this current increases regularly with thickness (t_f) in the range 0- 90nm (zone a). It varies slightly when the thickness varies from 100 nm to 200 nm, and decreases moderately when t_f is higher than 200 nm

We notice that the level of I_G is between 1E-11and 1E-9A, it is relatively high but can be explained if we consider the strong densities of intergranular traps in the polycrystalline layer. In the following, we will try to explain this behavior of I_G versus film thickness. The current I_G is assisted by the electric field. Its variation as a function of gate voltage is related to a POOLE –FRENKEL effect[2], which consists of an amplification of thermal generation by local electric field.

In order to explain the behaviour of the reverse current in a p-n polycrystalline silicon junction, GREVE [3] used the expression:

$$I_G \sim N_T W(t_f, V_{GS}) \exp\left(\frac{E(t_f, V_{GS})}{E_0}\right)^{1/2} \qquad (1)$$

Where:

I_G is the generation current

N_T is the intergranular traps density.

$W(t_f, V_{GS})$ is the extension of emission zone

$\left(\frac{E(t_f, V_{GS})}{E_0}\right)^{1/2}$ term which indicates an amplification of thermal coefficients

t_f is the film thickness

V_{GS} is the gate voltage

E_0 is the threshold field, its value is about 1E4 V.cm $^{-1}$ at T = 300K°.

4 – Geometrical model and Simulation

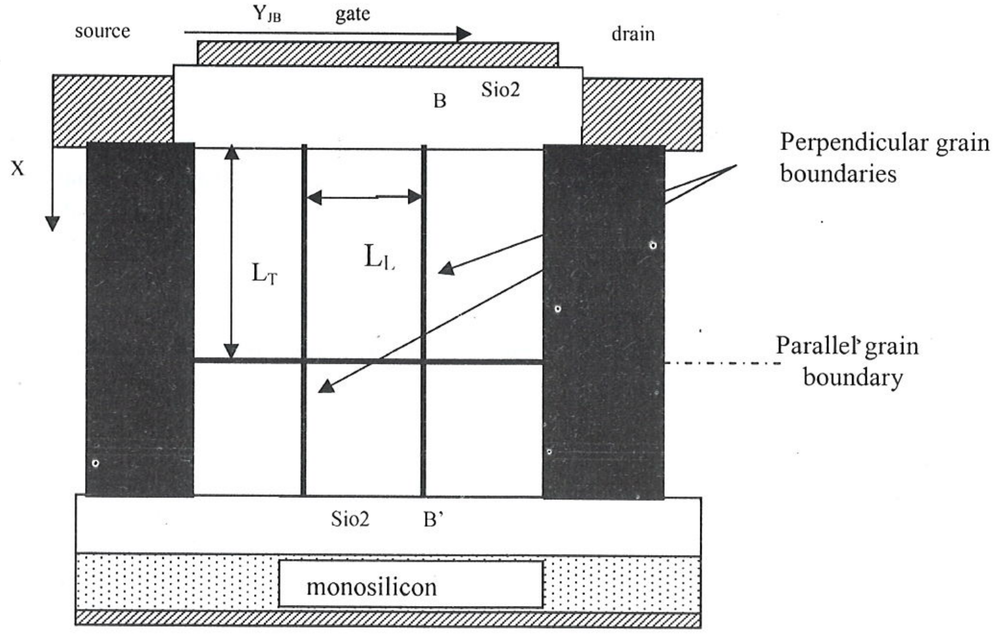

Fig 4:Geometrical model of the studied structure

The computation takes into account the electrical properties of polysilicon: monoenergetic traps are supposed to be uniformily distributed at the grain boundaries which are assumed as parallel and perpendicular to the interfaces, with a thickness equal to 1nm [4].Traps can be acceptors, donors or amphoteres[5,6]when the energetic levels E_{TA} and E_{TD} are symmetrically located at the midgap[7]. The size of the grains L_T in the tranverse direction is variable according to the thickness: it is the variable of simulation.

Based on GREVE's model, We will use the geometrical model shown in fig(4), in order to explain the behavior of current I_G versus film thickness. The space charge region of the grain boundary near the drain, being the principal zone of emission [1], so we try to calculate the electric field E_{yjb}, in the Y direction along BB' axis, in presence and the absence of a parallel grain boundary, using Poisson's equation which is defined as:

$$div\varepsilon grad\varphi = -q\left(p - n - N_A^- + N_D^+ - N_{TA}^- + N_{TD}^+\right) \qquad (2)$$

Where φ is the electrostatic potential, ε the silicon dielectric constant, n, p the free carrier concentration, N_D^+ and N_A^- are concentrations of the ionized doping atoms, N_{TA}^- and N_{TD}^+ are concentrations of the ionized traps.

Partial differential equation (2) is discretized by the use of the finite differences method [8] which is easy to solve by the direct method of Gauss. At the end, the electric field E_{yjb} is calculated. Indeed, the intensity of this one varies according to the position of the point in the layer thickness. Thus, we notice that the effect of this field is :

1 to extend to the whole film thickness at low thicknesses fig (5).

2 restricted only to the higher part of the polycrystalline layer for the great thicknesses fig (6).

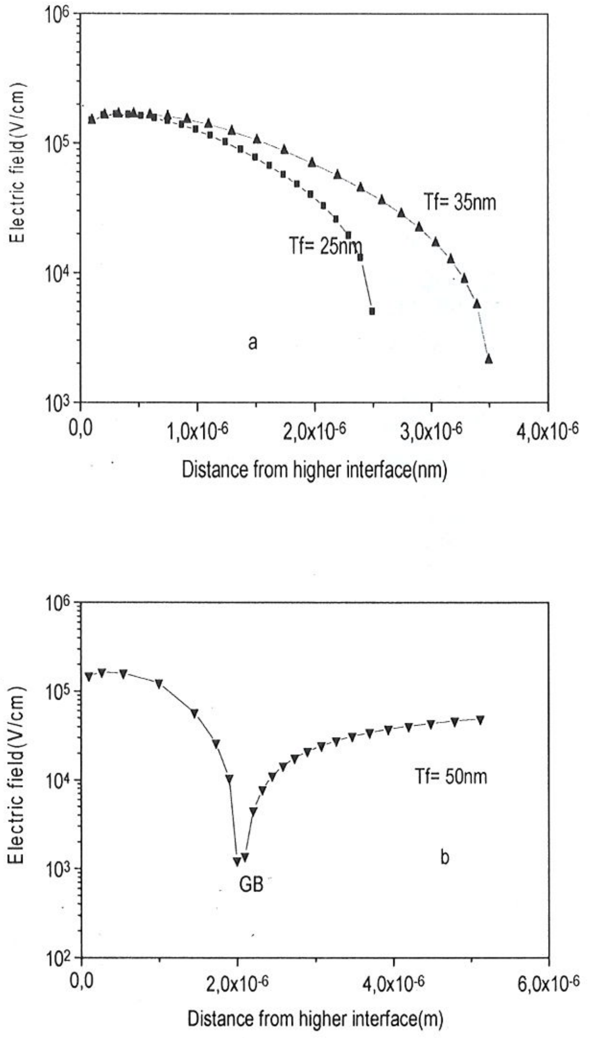

Fig 5: intensity of the electric field for two film thicknesses

a) in the absence of parallel grain boundary

b) in the presence of the grain boundary localized at 20nm from higher interface

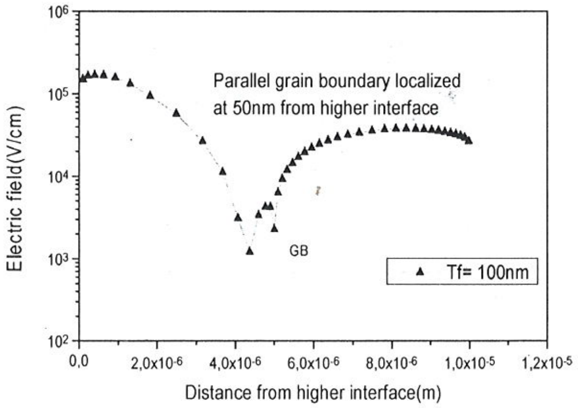

Fig 6: intensity of the electric field in the presence of the parallel grain boundary localized at 50 nm from higher interface.

The shape of the curves depends obviously on the coupling between the gate charge and the trapped charge at the grain boundary (or back interface). As the side size of the grains and the density of the traps play a fundamental role in the effectiveness of this coupling [9], we will carry out simulations for various side sizes L_L and various densities of traps N_T.

4.1-calculation of the average field and the extension of the emission zone

The precedent curves are not directly exploited, we defined an average field E_{av} and an effective emission zone W.

The average field is defined by:

$$E_{av} = \frac{\int_0^W E(x,y_{JB})dx}{\int_0^W dx} = \frac{\sum E(x,y_{JB})\Delta x}{W} \qquad (3)$$

Where W is the zone where the electric field is sufficiently important $E_{av} > E_o = 1E4Vcm^{-1}$ to amplify the thermal emission. The average field and the emission zone, versus film thickness are shown in fig (7), for various L_L, N_T doping and gate bias are fixed to $2e12cm^{-2}, 1e17cm^{-3}$ and 5V respectively, when a parallel grain boundary is localized at 70nm from the back interface.

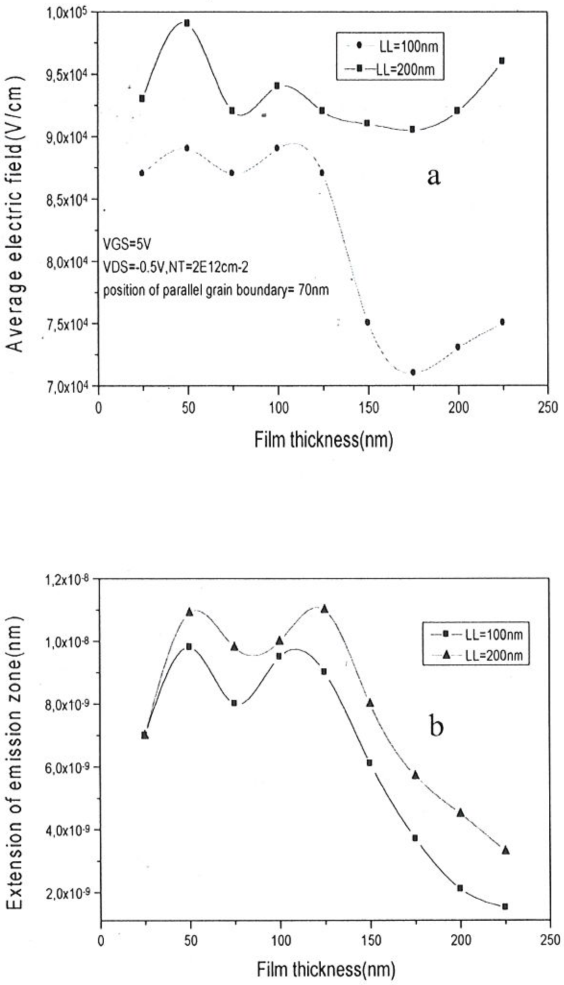

Fig7: Average electric field (a) and extension of the emission zone (b) versus film thickness for two grain side sizes

Comments

the intensity of the average field varies between 7E 4 and 1E 5 V cm $^{-1}$, this values are sufficient value to amplify the thermal emission . the evolution of E_{av}, and W depend strongly on the side size of the grains L_L: in the all range of studied thickness, the intensity of the average field and W increase with L_L. The generation current being proportional to the product definite by:

$$P = W \exp\left(\frac{E_{av}}{E_0}\right)^{1/2} \qquad (4)$$

We will calculate this product for all the range thickness. Fig 8 shows that P presents a similar evolution to $I_G(t_f)$ only when the thickness layer is superior than 100nm.

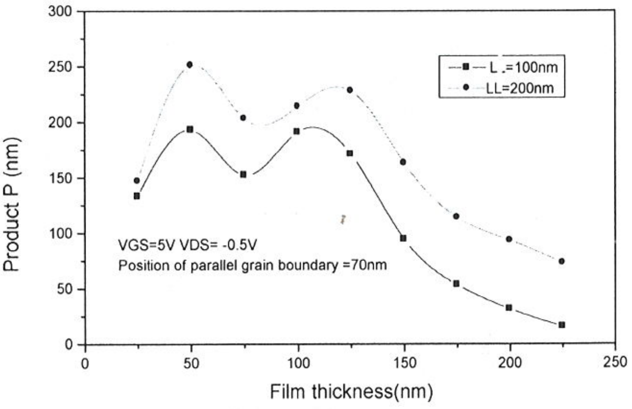

Fig 8: Product P versus film thickness calculated for two grain sizes

4.2- Effect of a density traps variation on $P(t_f)$

Thus, we tried to see the effect of a variation of intergranular traps density on $P(t_f)$. Fig (9) illustrates this variation for a side size L_L equal to 200 nm. For low thicknesses and the small gate voltage ,$P(t_f)$ increases with N_T . The simulation demonstrated that the density of intergranular traps does not modify the shape of $P(t_f)$, but it affects the value of the product P.

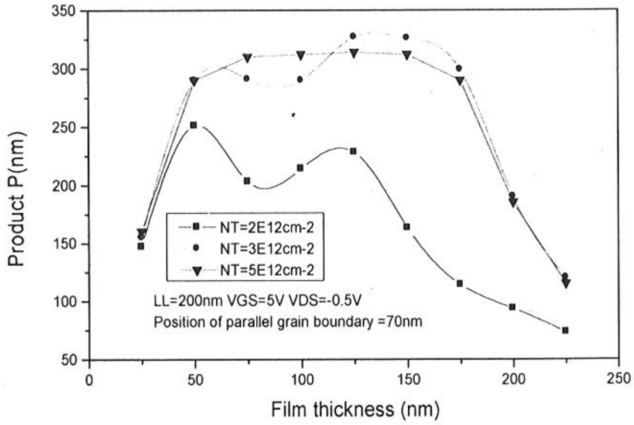

Fig 9: product P versus polycrystalline layer thickness for various intergranular traps density

4.3- Adjustment of the generation current and the product P

The analysis of the variation of the product P according to the thickness of the polycrystalline silicon layer and the gate voltage makes it possible to adjust the evolution of P (t_f) to that of I_G (t_f) (fig (11)), while considering:

- $L_L = 200$ n m and $N_T = 1E12cm^{-2}$
- Parallel grain boundary is localized at 110 n m from the back interface

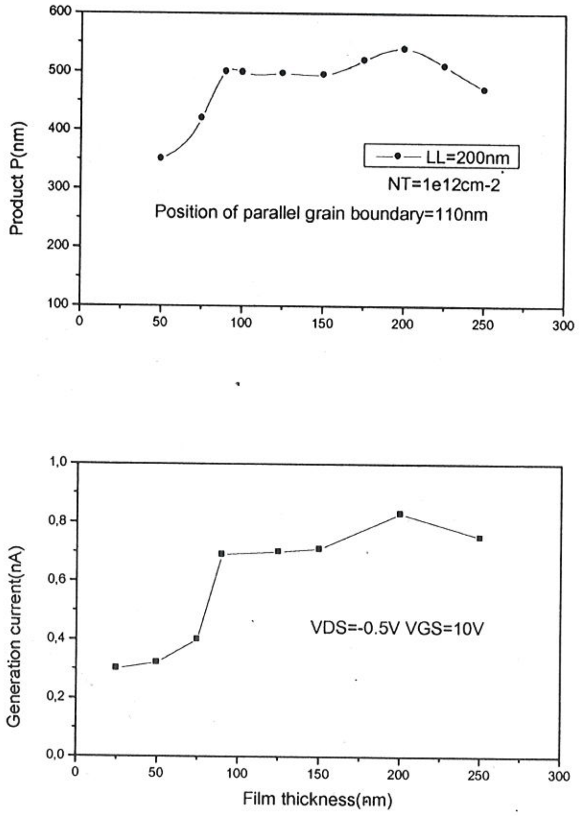

Fig 10: simultaneous variation as a function of film thickness of $I_G(t_f)$ and $P(t_f)$, With a grain sizes equal to 200nm and intergranular traps density fixed to $1e12cm^{-2}$

the value of the grain sizes and the position chosen for parallel grain boundary during the adjustment of $I_G(t_f)$ and $P(t_f)$ are in conformity with the micrographic observations.

On the one hand, this simulation permits us to obtain the form of $I_G(t_f, V_{GS})$, but on the other hand, we don't find the level of generation the current. Indeed, other parameters such as the density of traps, or the emission coefficients in the absence of field, also determine the level of this current

5- Conclusion

This analysis of the generation current according to the thickness of the polycrystalline layer and the gate voltage shows that the parallel grain boundary plays a fundamental role in the variation of I_G versus film thickness. When the side size of the grains increases the intensity of the average field becomes important and sufficient to amplify the thermal emission. If we reduce N_T , the generation current I_G decreases, not only by reduction of the density of intergranular traps, but by reduction of the rate of amplification of the emission coefficients.

The electrostatic coupling of the interfaces, or the higher interface and a parallel grain boundary is a fundamental electrostatic phenomenon for the interpretation of the evolution of the generation current according to the thickness of film. However, It is him even influenced by the existence of the perpendicular grain boundaries and thus, depends on the grain sizes, the doping, and on density of intergranular traps. this study inform us on the optimal thickness to choose in order to optimize the performances of polysilicon MOS transistors. This work can be continued by carrying out a similar modelling using another granular aspect of the active layer.

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SYMBOLS TABLE USED IN THE SIMULATION MODEL

-I_G	-generation current
-t_f	-film thickness
-V_{GS}	-gate voltage
-N_T	-intergranular traps density.
-W	-the extension of emission zone
-Eo	- the threshold field
-$\exp(E(t_f,V_{GS})/Eo)$ ½	-term indicating an amplification of the thermal coefficients
-q	-electron charge
-φ	-the electrostatic potential
-ε	-the silicon dielectric permittivity
-n, p	-the free carrier concentration
-N_D^+, N_A^-	- the ionized doping densities
-N_{TA}^-, N_{TD}^+	-the concentrations of the ionized traps.
-E_{yjb}	-the electric field in the Y direction
-E_{av}	-the average field.
-L_T	-the grain size in the transverse direction.
-L_L	-the grain side size.
-P	-the product.