Current transportin Au/SPAN/n-GaAs structures from Current-Voltage-Temperature characteristics

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Keywords

I–V-T characteristics, Current transport, Gaussian distribution (GD),Schottky barrier diode,SPAN.

Abstract

Current–voltage (I–V) characteristics of Au/SPAN/n-GaAs Schottky barrier diodes(SBDs) have been investigated in the wide temperature range of 80–300 K. Zero-bias barrier height (Φ_{B0}) and ideality factor (n) are temperature dependent, withΦ_{B0} increasing and n decreasing with increasing temperature. Φ_{B0} versus n, and (n^{-1}-1) versus q/2kT plots were drawn to obtain an evidence of Gaussian distribution (GD) of interface Barrier Heights.Plots show relatively important standard deviation values that indicate interface inhomogeneities and complex current transport through the interface.Temperature dependent I–V characteristics of Au/SPAN/n-GaAs SBDs have successfully explained current transport in these devices. It is concluded that current transport is TE dominated with double-Gaussian distribution of SBHs rather than other mechanisms.

1. Introduction

Electrical characteristics of metal-semiconductor (M-S) and metal-insulator/polymer-semiconductor (MIS/MPS) Schottky barrier diodes (SBDs) continue to be widely examined because of their importance in the field of electronic and optoelectronic applications**[1,2].**Barrier height (BH) formation in these diodes isrelated to various structure parameters such as interfacial layer at M/S interface , series and shunt resistances (R_s and R_{sh}), density of interface states (Nss), doping acceptor/donor atoms concentration, homogeneity of barrier height (BH),applied bias voltage and sample temperature**[3].**The use of an organic layer can

givesome advantages such as light weight, low cost, flexibility and easein fabrication. In addition, such organic interfacial layer on inorganic material such as GaAs can minimize interface traps density, dislocations, Rs and increase rectification rate and R_{sh}**[4].**
There are many conjugated polymers that can be used as interfacial layer such as PVA **[5],**polyindole**[6]** and perylene**[7]**. In addition, conjugated polymers such as polyaniline (PANI), poly (p-phenylene-vinylene), polypyrrole, polyacetylene, polythiophene, sulfonated polyaniline (SPAN), etc.,are used in hybrid organic/inorganic devices,and show intriguing conducting properties[8]. SPAN is one of such interestingconducting polymers that has unusual electro-active physical properties, improved process-ability, and potential industrial applications **[9].** SPAN is used in making multilayer hetero-structure light emitting diodes**[10]** and films electrodes for battery applications**[11].** This material is also being used in electronic circuitry design**[1]**.
Growth and characterization of conducting polymer layers on GaAs, and the nature of BH that result at interface, still remains afundamental issue. The popularity of such studies is attached in their importance to the interfacial polymer layer in Metal-Polymer-Semiconductor diode**[12]**. Experimental results found at room temperature don't give detailed information on current conduction mechanisms and barrier formation at M-S interface. Taking I–V characteristics on a wide temperature range enables one to comprehend distinctive parts of conduction mechanisms and device properties.In this study, temperature dependent forward bias I–V characteristics of Au/SPAN/n-GaAs SBD are investigated fortemperatures rangefrom80K to 300K. Dependence of BH and n on temperature is determined. Such behavior of ϕ_{B0} and n with temperature is explained by assuming of double Gaussian distribution (GD) of BHs due to barrier inhomogeneities that usually prevail at M/S interface.

2. Device structure

Device are made of n-type silicon doped GaAs substrates, with 2×10^{18} cm^{-3} dopant concentrations, on which are grown SPAN thin films having thickness of about 200 µm by self-assembly at a rate of 1.8 nm/h. SPAN orientation growth has been initiated on (311)B

GaAs substrates. Prior to SPAN growth process and after cleaning process of substrates, nickel (Ni)-gold (Au) was evaporated onto the whole back side of the wafer in a vacuum system to make ohmic contacts. Finally, 0.0020 cm^2 circular electrical contacts were obtained by thermal evaporation of 99.99% pure Au on SPAN films. **Fig.1** shows a typical structure of investigated Au/SPAN/n-GaAs organic-inorganic Schottky devices.

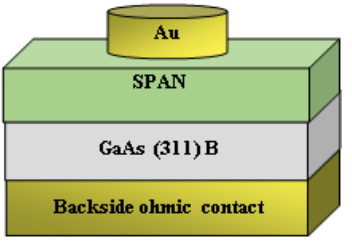

Fig.1: Schematic diagram of fabricated Au/SPAN/n-GaAs Schottky Barrier Diodes.

While changing temperature, current–voltage (I–V) characteristics of Au/SPAN/n-GaAs SBDs were measured using an Agilent precision semiconductor parameters analyzer (4156C). Temperature was increased from 80K to 300K with a step of 10 K in a cryostatusing a Lakeshore 336 temperature controller.

3. Results and discussion

3.1 Barrier height and ideality factor temperature dependence

Fig.2 shows forward bias I–V characteristics of Au/SPAN/n-GaAs SBD, measured over temperature range 80K to 300K. According to TE theory, the relation between I and V in forward bias region ($V \geq 3kT/q$) for a SBD is given by**[2]:**

$$I = \underbrace{A\,A^{*}T^{2}\exp\left(-\frac{q\Phi_{B0}}{kT}\right)}_{I_0}\left(\exp\frac{qV}{nkT}-1\right) \qquad (1)$$

Where,pre-factor of equation (1) is the reverse saturation current (I_o), A is rectifier contact area, A* is Richardson constant (8.16

A/cm^{-2}K^{-2} for n-type GaAs) **[13],** T is temperature in K, V is forward-bias voltage, n is ideality factor.

From equation (1), ideality factor n can be written as:

$$n = \frac{kT}{q}\, ln\left(\frac{d(V)}{d\, ln\, I}\right) \qquad (2)$$

The value of Φ_{B0} is obtained using **[4]:**

$$\phi_{B0} = \frac{kT}{q} \ln\left(\frac{AA^{*}T^{2}}{I_0}\right) \qquad (3)$$

Temperature dependence of experimental values of I_o, n, Rs and $\phi_{B0}$of Au/SPAN/n-GaAs SBD is shown in **Tab.1**. **Fig.3**shows how ϕ_{B0} increases and n decreases with increasing temperature. It is clear that both the values of n and ϕ_{B0} are strong functions of temperature.As can be seen from **Tab.1**, I_0 and ϕ_{B0} increase with increasing temperature, while n and R_s decrease with increasing temperature.

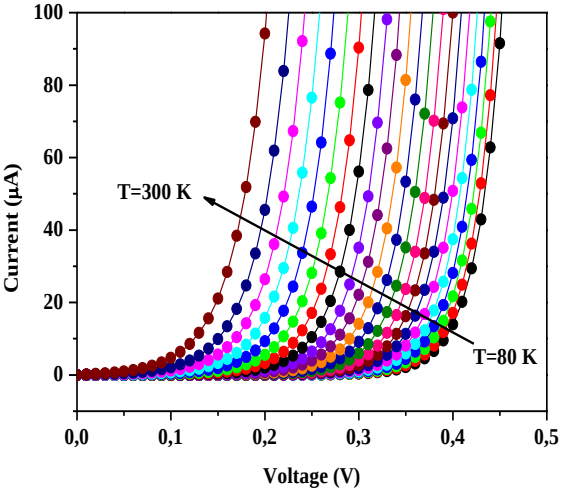

Fig.2: I-V-T characteristics of Au/SPAN/n-GaAs Schottky diodes.

Tab.1 Temperature dependence of I_o, n, $\phi_{B0}$and Rs for Au/SPAN/n-GaAs SBD

T (K)	I_0 (A)	n	ϕ_{B0} (eV)	Rs (Ω)
80	7,40 X 10^{-12}	4,03	0,20	2310,63

120	2,12 X 10^{-11}	2,70	0,31	931,83
160	9,54 X 10^{-11}	2,04	0,40	307,21
200	7,07 X 10^{-10}	1,60	0,50	108,71
240	7,92 X 10^{-9}	1,41	0,55	48,67
280	1,38 X 10^{-8}	1,35	0,57	26,71
300	1,00 X 10^{-8}	1.26	0.60	1,53

From **Fig.3**, ϕ_{B0} increase with increasing temperatureshowing that current transport across the M/S interface is temperature activated process. That is, electrons at low temperatures are able to surmount lower barriers at some interface patches and therefore current conduction will be dominated by current flowing through lower barriers and leads to high values of n **[6,14,15]**. Hence, n value is very high at low temperature and decrease almost exponentially with increasing temperature. This high value of ideality factor has been attributed to polymer layer (SPAN) at metal/semiconductor interface and particular distribution of interface states localized at semiconductor/conducting polymer (GaAs/SPAN) interface **[4,15].** Similar results have been reported in literature for other Schottky structures **[6,14].**

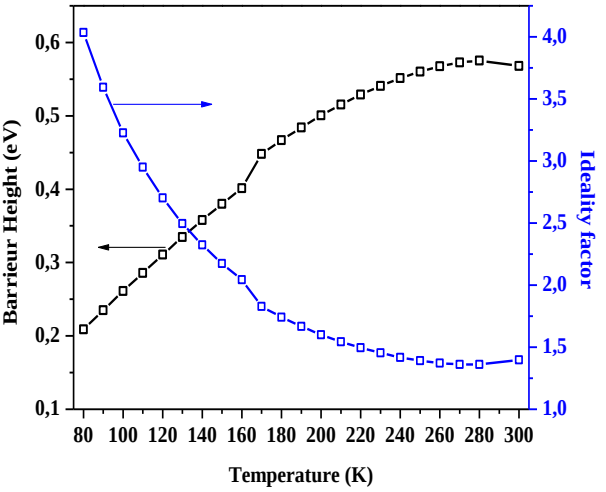

Fig.3:Variation in ideality factorand zero-bias barrier height with temperature.

3.2 Ideality factor and T_0 effect

At many M/S interfaces, ideality factor of a diode is known to increase when sample temperature is brought down. Such behavior of n with temperature has lead workers to find its value at 0K, which is known as the "T_0 effect" or "T_0 anomaly" **[16,17]. Fig.4** shows the behavior of n versus 1000/T.As can be seen, n increases with decreasing temperature and shows linear temperature dependence that can be expressed as:

$$n(T) = n_0 + \frac{T_0}{T} \qquad (4)$$

where n_0 and T_0 are constants thatare found from intercept and slope. They are 0.08 and 313 K, respectively. Such ideality factor behavior suggests that tunneling current mechanisms such as Thermal Field Emission (TFE) or possibly Field Emission (FE) have to be taken into consideration besides Thermal Emission (TE).

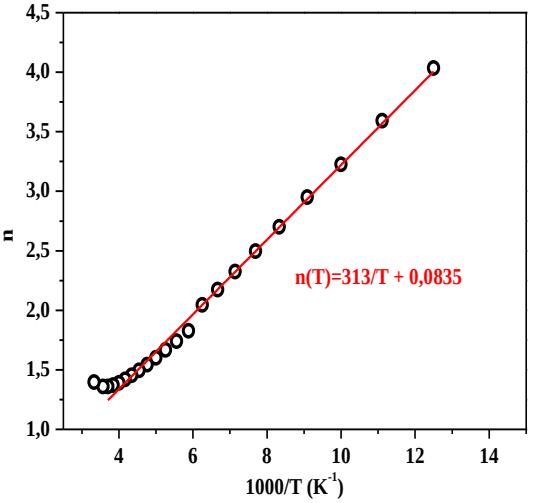

Fig.4 : n versus 1000/T plot. The values of n_0 and T_0 are shown in figure.

3.3 Barrier height distribution

Decrease in BH with the decrease in temperature suggests a lateral distribution of BH. Let consider a Gaussian distribution of BHs over

Schottky contact area with mean BH value $\overline{\phi_{B0}}$ and standard deviation σ_s . Here, standard deviation is a measure of barrier homogeneity. This Gaussian distribution of BHs is given by **[18,19]:**

$$\phi_{B0} = \overline{\phi_{B0}} - \frac{q{\sigma_s}^2}{2kT} \qquad (5)$$

Temperature dependence of σ_s is usually small and can be neglected. Observed variation of apparent ideality factor with temperature in this model is given by **[18,19]:**

$$\left(\frac{1}{n_{ap}} - 1\right) = -\rho_2 + \frac{q\rho_3}{2kT} \qquad (6)$$

where ρ_2 and $\rho_3$quantities are voltage coefficients which may depend on temperature and then quantify voltage deformation of BH distribution. It is assumed that mean Schottky barrier height $\overline{\phi_{B0}}$ and σ_s are linearly bias dependent on Gaussian parameters, such as $\overline{\phi_{B0}} = \phi_{B0} + \rho_2 V$ and standard deviation $\sigma_s = \sigma_{s0} + \rho_3 V$.
Fig.5 shows variation of ϕ_{B0}as a function of n for Au/SPAN/n-GaAs. Barrier height is correlated linearly with ideality factor with an extrapolated ϕ_{B0}at n = 1 that would correspond to the laterally homogeneous barrier height and for which pure TE applies as the unique mechanism through which conduction takes place. ϕ_{B0}versus n characteristics show twolinear regions over two temperature ranges (300–140 K) and (130–80 K).The two extrapolated barrier heights at n = 1 are 0.66 eV and 0.46 eV, for the first and second region respectively.

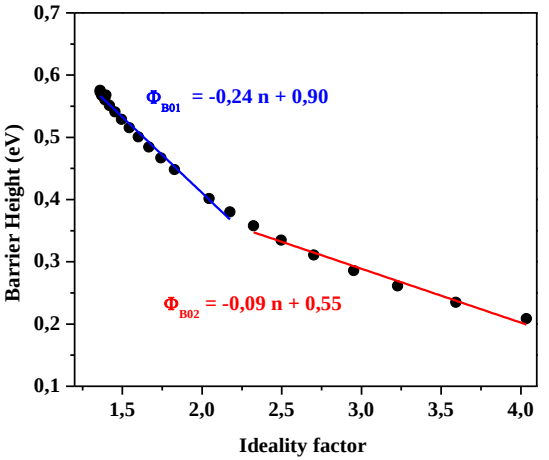

Fig.5: ϕ_{B0} versus n plot for Au/SPAN/n-GaAs SBD in 80-300 K temperature range.

Fig.6showsϕ_{B0} versus q/2kT plotthat should be a straight-line with intercept at the ordinate determining zero-bias mean BH $\overline{\phi_{B0}}$ and slope giving zero-bias standard deviation σ_s. Experimental ϕ_{B0} versus q/2kT plots,Fig.6, have two linear regions indicating two types of barriers at least. Since current transport across the diode is a temperature activated process, electrons at low temperatures are able to surmount lower barriers and therefore current transport will be dominated by current flowing through patches of lower SBH corresponding to larger ideality factors. However, as temperature increases, more and more electrons have sufficient energy to surmount higher barriers. In this case, ideality factor value is closer to unity and for these high temperatures TE becomes the predominant mechanism. As a result, dominant barrier height will increase with temperature and bias voltage. Above observations indicate the presence of at least two Gaussian distribution of barrier heights in contact area.

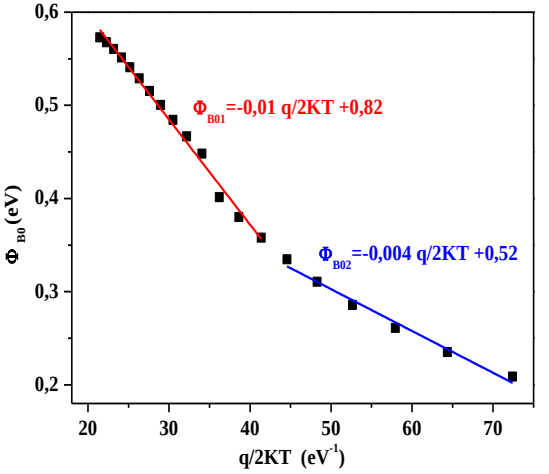

Fig.6: Zero-bias barrier height vs. q/2kT plot of Au/SPAN/n-GaAs SBDs.

Intercepts and slopes of straight-lines of Fig.6 give two sets of values for $\overline{\phi_{B0}}$ and σ_s : (0.82 eV ; 0.1V) in temperature range 300K-140K, and (0.52 eV ; 0.063V) in temperature range 130K-80K. Standard deviation is a measure of barrier homogeneity with lower values corresponding to more homogenous barrier heights. Hence, above values of $\sigma_s$being relatively important indicate the presence of interface inhomogeneities that can be attributed to variation in interface composition/phase, interface fabrication quality, electrical charges, non-stoichiometry, etc. They are important enough to electrically influence current-voltage (I–V) characteristics of Schottky diodes, at particularly low temperatures**[18].**Thus, I–V measurements at very low temperatures are capable of revealing the nature of barrier inhomogeneities present in contact area. Existence of second Gaussian distribution at very low temperatures may possibly arise due to some phase change taking place on cooling below a certain temperature. Furthermore, temperature range covered by each straight-line suggests the regime where corresponding distributionsare effective.

Two barrier height distributions can also be seen when plotting (n^{-1}-1) versus q/2kT,**Fig.7**. Intercept and slope of straight-lines in this plot give voltage coefficientsρ_2 and ρ_3, respectively. Obtained values of ρ_2 are -0.09 (distribution 1), and 0.36 (distribution 2), whereas values of ρ_3 are 0.01V and 0.005V, respectively. The linear behavior of this plot demonstrates that ideality factor does indeed express voltage deformation of Gaussian distribution of SBH. As can be seen from the plot, ρ_3 value or slope of distribution 1 is larger than distribution 2, therefore we may point out that distribution 1 is a wider and relatively higher barrier height with bias coefficients ρ_2 and ρ_3 being smaller and larger, respectively.

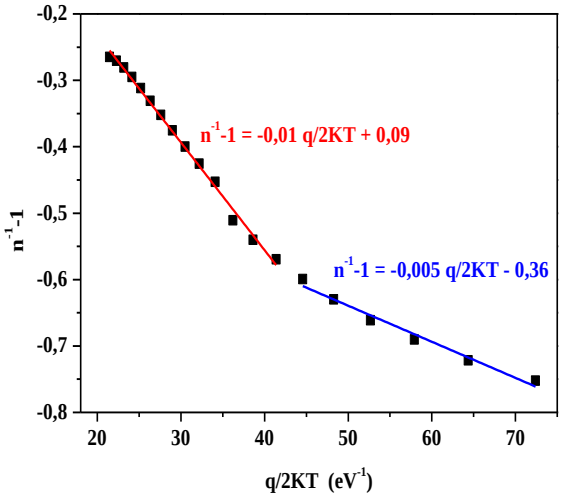

Fig.7: (n^{-1}-1) versus q/2kT plot of Au/SPAN/n-GaAs SBD in 80–300 K range.

4. Conclusion

Forward bias I–V characteristics of Au/SPAN/n-GaAs Schottky diode have been investigated over wide 80–300 K temperature range. Main diode parameters such as Io, n, ϕ_{B0} and Rs values were calculated foreach temperature value.Estimated ϕ_{B0} and n, assuming TE mechanism, show strong temperature dependence. While n decreases, ϕ_{B0} increases with increasing temperature. In order to explain this unexpected behavior of ϕ_{B0}, ϕ_{B0} versus n, and (n^{-1}-1) versus q/2kT plots were drawn to obtain an evidence of a

Gaussian distribution (GD) of BHs fortwo temperature regions. From theses plots, values of σ_s being relatively important indicate the presence of interface inhomogeneities and the linear behavior of plots demonstrate that ideality factor does indeed express voltage deformation of Gaussian distribution of SBH. It is concluded that temperature dependent I–V characteristics of Au/SPAN/n-GaAs SBDs can successfully explain that current transport in these devices is dominated by TE mechanism with double-Gaussian distribution of SBHs rather than other mechanisms.

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