Electrical and Interface properties of MBE grown Fe/n-$Si_{0.85}Ge_{0.15}$ (111) Schottky Barrier diodes

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Abstract: *Current–voltage characteristics of (111) oriented Fe/n-$Si_{0.85}Ge_{0.15}$ metal–semiconductor Schottky barrier diode, deposed by Molecular Beam Epitaxy, are investigated at room temperature. Using thermionic emission theory, forward bias* I–V *characteristics are analyzed to estimate Schottky diode parameters. Electrical parameters, such as ideality factor, zero-bias barrier height and series resistance are calculated using two different methods. Results show three distinct linear regions in ln(I)–ln(V) plots, indicating ohmic, trap-charge limited current and space-charge limited-current conduction mechanisms. Energy distribution of interface states was obtained from forward bias* I–V *measurements by taking into account bias dependence of effective barrier height and ideality factor. I-V characteristics confirmed that series resistance distribution and interfacial layer formation are important parameters that influence electrical properties of device.*

Keywords: Electrical characterization / I-V measurement / Fe-$Si_{1-x}Ge_x$ / Schottky diode / N_{SS} Energy dependence.

résumé: *Les caractéristiques courant-tension d'une diode métal-semi-conducteur de type Schottky (111) Fe/n-$Si_{0.85}Ge_{0.15}$, déposée par Epitaxie à Jet Moléculaire, sont étudiées à température ambiante. En utilisant la théorie de l'émission thermoïnique, les caractéristiques I-V en polarisation directe sont analysées pour estimer les paramètres de la diode Schottky. Les paramètres électriques, tels que le facteur d'idéalité, la hauteur de la barrière à polarisation nulle et la résistance en série, sont calculés selon deux méthodes différentes. Les résultats montrent trois régions linéaires distinctes sur les courbes ln(I)-ln(V), indiquant trois mécanismes de conduction: Ohmique, courant limité par capture et courant limité par charge d'espace. La distribution d'énergie des états d'interface a été obtenue à partir des mesures I-V en polarisation directe en prenant en compte la dépendance sur la polarisation de la hauteur de barrière efficace et du facteur d'idéalité. Les caractéristiques I-V ont confirmé que la distribution de la résistance en série et la formation d'une couche à l'interface sont des paramètres importants qui influencent les propriétés électriques du dispositif.*

Mots clés: Caractérisation électrique / Mesure I-V / Diode Schottky / Fe-$Si_{1-x}Ge_x$ / dépendance énergétique de N_{SS}.

1. Introduction:

$Si_{1-x}Ge_x$/Si heterostructures are of great interest because of their potential use as heterojunction devices and their compatibility with Si integrated circuit technology [1, 2]. Band gap engineering of strained $Si_{1-x}Ge_x$ epitaxial layer by changing Ge fraction makes this material suitable for a wide variety of electronic device applications [3]. Metallization in device fabrication is also important for electrical evaluation of metal-semiconductor interfaces and semiconductors. Hence, the study of this Schottky contact for different metals and under various conditions is useful for achieving a better understanding and control of electrical characteristics. Transport mechanisms in Schottky barrier diodes (SBD) have been extensively studied both experimentally and theoretically. Carrier transport in these structures is known to be dominated by thermionic emission. There are, however, discrepancies constantly reported between experimental data and theoretical models, especially with respect to Schottky–Mott theory [4] developed to explain SBDs formation mechanism. These deviations have been attributed, in the literature, to various reasons [5–9], including the existence of interface states spread over a thin interfacial layer between the metal and semiconductor, and metal induced gap states, which could result in non-uniform spatial distribution of barrier height [10].

The purpose of this paper is to study current–voltage (I–V) characteristics of Fe/n-$Si_{0.85}Ge_{0.15}$ Schottky diodes to extract diodes parameters at room temperature and attempt to explain their behavior considering possible conduction mechanisms. Iron (Fe) has been used because of its good physical characteristics. Schottky Barrier Height (SBH), ideality factor (n) and series resistance (R_s) have been calculated using Norde method. Log-log I-V plots are used to evaluate existing mechanism transport.

2. Experimental details

Fe/n-$Si_{0.85}Ge_{0.15}$ Schottky diodes fabrication started with a molecular beam epitaxy (MBE) growth, at a substrate temperature of 550°C, of n-type (111) oriented $Si_{0.85}Ge_{0.15}$ films doped with Antimony (N_D =3-4×$10^{15}cm^{-3}$). Film thickness was 2µm on 350µm thick (111) crystal orientated Si substrats having ≅0.7 Ω.cm resistivity. $Si_{0.85}Ge_{0.15}$ wafers were degreased in organic solvent (HF- HNO_3- CH_3COOH and CH_3OH)

and etched in a sequence of H_2SO_4 and H_2O_2, 20% HF, a solution of $6HNO_3$: 1HF: $35H_2O$, 20% HF and finally quenched in de-ionized water of resistivity 18MΩ.cm. Immediately after surface cleaning, high purity (99.999%) Fe circular contact, 1.3mm in diameter and ~0.2μm in thickness were thermally evaporated onto $Si_{0.85}Ge_{0.15}$ film. The high vacuum metal evaporation system had a pressure about 10^{-6} Torr. Low resistivity ohmic back metal contact was obtained with Al metallization of wafer back-side.

Current–voltage (I-V) and capacitance–voltage (C-V) measurements of devices were performed using an Agilent precision semiconductor parameters analyzer (4156C) and an Agilent LCR meter (4980A).

3. Results and discussion:

Current- voltage characteristics are widely used to study Schottky contacts performance since they offer many important device parameters. Fig.1 shows forward and reverse biased curves of Fe/n-$Si_{0.85}Ge_{0.15}$ (MS) Schottky diodes at room temperature. Diode rectifier rate (RR), deduced from Fig.1, is 5.65×10^2 at V=±0.4V. It is clear that forward bias I-V plot deviates considerably from linearity at high bias voltage due to R_s reinforced by a possible interfacial layer. Leakage current at -1V bias is 1.6×10^{-7}A. For forward bias V>3kT/q, Schottky's I-V characteristics obey thermionic emission theory according to the following equation [16, 26]:

$$I = I_S \exp\left(-\frac{q(V-IR_S)}{nkT}\right) \qquad (1)$$

Where I_S is saturation current given by:

$$I_S = AA^*T^2 \exp\left(-\frac{q\phi_{B0}}{kT}\right) \qquad (2)$$

Where A is contact area, T is temperature in [K], $A^*$is Richardson constant (taking an effective mass of $0.22m_e$ for $Si_{0.85}Ge_{0.15}$, calculated A^* value is $112Acm^{-2}K^{-2}$), ϕ_{B0} is zero bias barrier height, k is Boltzmann constant, R_s is the series resistance and n is the ideality factor. Ideality factor can be determined from the slope of linear region of forward bias lnI-V curve using the relation [16]:

$$n = \frac{q}{kT}\frac{dV}{d(\ln I)} \qquad (3)$$

ϕ_{B0} and n values of Fe/n-$Si_{85}Ge_{15}$ diode were calculated from equation (2) and equation (3) and found to be 0.749 eV and 1.92, respectively. It is clear that n value is considerably larger than unity. This high value of n is

attributed to the existence of an interfacial layer with a certain density distribution of interface states (N_{SS}) [11-14, 16]. Norde proposed an empirical function to calculate barrier height and series resistance for a Schottky diode [15]. Such function is defined as:

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\ln\left(\frac{I(V)}{AA^*T^2}\right) \qquad (4)$$

where γ is a dimensionless integer greater than ideality factor, and I(V) is current obtained from forward bias I-V plots. Norde basic technique is to plot the above function with respect to applied voltage and to obtain its minimum. Once the minimum of F(V) versus V is found, barrier height value can be obtained using the following equation:

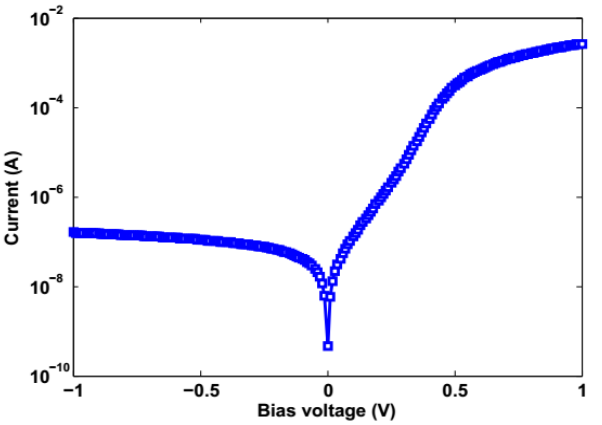

Fig.1. I-V characteristics of Fe/n-$Si_{85}Ge_{15}$ Schottky diode.

$$\phi_B = F(V_{min}) + \frac{V_{min}}{\gamma} - \frac{kT}{q} \qquad (5)$$

where $F(V_{min})$, V_{min}, and I_{min} are minimum values of F(V), corresponding voltage and current, respectively. From Norde function, series resistance value can be determined using the following equation:

$$R_S = \frac{kT(\gamma - n)}{qI_{min}} \qquad (6)$$

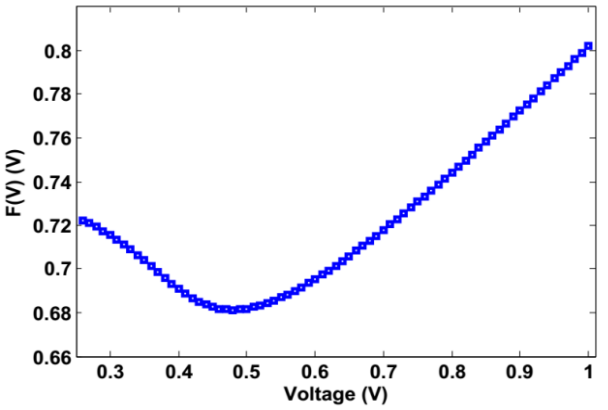

Fig.2. F(V) vs. V plot of Fe/n-$Si_{0.85}Ge_{0.15}$ Schottky diodes.

Fig.2 shows F(V) versus V plot for Fe/n-$Si_{0.85}Ge_{0.15}$ SBD. Barrier height and series resistance extracted from this plot are 0.82eV and 87Ω, respectively. As shown in table (1), there is a good agreement between barrier height, ideality factor and series resistance values extracted using I-V and Norde methods. Hence, mean values for Fe/n-$Si_{0.85}Ge_{0.15}$ diode are R_s=86±1.1Ω, ϕ_{B0}=0.79±0.04eV.

Table (1) Some important Fe/n-$Si_{0.85}Ge_{0.15}$ diode parameters

	Ideality factor	Barrier Height (eV)	Series resistance Rs (Ω)
I-V	2	0.749	84.85
Norde		0.829	87.11

To obtain information about the contact interface of SBDs, C-V measurements are used. Moreover, this technique is reliable to estimate barrier height. Fig.3 shows the $1/C^2$-V plot of Fe/n-$Si_{0.85}Ge_{0.15}$ interface measured at the frequency of 1MHz. The straight line is consistent with Schottky- Mott model, which assumes that the carrier concentration is constant through the depletion width of the Schottky junction. C-V relationship for Schottky diodes is given by [16]:

$$\frac{1}{C^2} = \left(\frac{2}{\varepsilon_S q N_D A^2}\right)\left(V_{bi} - \frac{kT}{q} - V\right) \qquad (7)$$

Where C is capacitance, A is area of Schottky contact and ε_s is the permittivity of semiconductor, N_D is the doping concentration, and V_{bi} is the built-in voltage. The x-axis intercept of the plot of $1/C^2$ versus V gives

V_0. V_0 is related to V_{bi} by the equation $V_{bi}=V_0+kT/q$. The barrier height from C-V characteristics is given by equation $\phi_B=V_{bi}-V_n$ where $Vn=(kT/q)\ln(N_C/N_D)$. N_C is the effective density of state in conduction band and is 2.3×10^{19} cm^{-3} for $Si_{0.85}Ge_{0.15}$ [16]. Doping concentration, calculated from the slope of $1/C^2$-V plot, was found to be 3.1×10^{15} cm^{-3} for Fe/n-$Si_{0.85}Ge_{0.15}$ diode. From $1/C^2$-V plot, barrier height was found to be 1.1eV. It should be noted that barrier height measured from $1/C^2$-V plot, is always higher than that derived from forward I-V characteristics. A relatively large discrepancy between barrier heights measured using I-V and C-V techniques could be associated with barrier height inhomogeneity at the Schottky interface.

To understand electrical transport mechanisms through the device, ln(I)-ln(V) plots are taken for forward bias. As can be seen in Fig.4, ln(I)-ln(V) plots have three distinct linear regions with different slopes. Region (1) spans 0.1V<V<0.15V, region (2) spans 0.16V<V<0.45V and region (3) spans 0.46V<V<1V. All three regions obey equation $I\propto V^m$. Here, m represents the slope of each linear region and found to be 1.52, 8.73 and 2.71, respectively. It is clear that current conduction at low bias, region (1), shows an almost ohmic behavior, that is, current is directly proportional to applied bias voltage [17, 18, 20]. On the other hand, in region (2), I-V relation is characterized by a power law. In this region, electrical transport behavior is dominated by trap-charge limited current (TCLC) with an exponent trap distribution [18,19]. In this case, injected electrons cause filling up of traps and change the space charge [37]. At strong forward bias, region (3), strong electron injection causes electrons to escape from traps and contribute to space-charge limited-current [18, 20, 21].

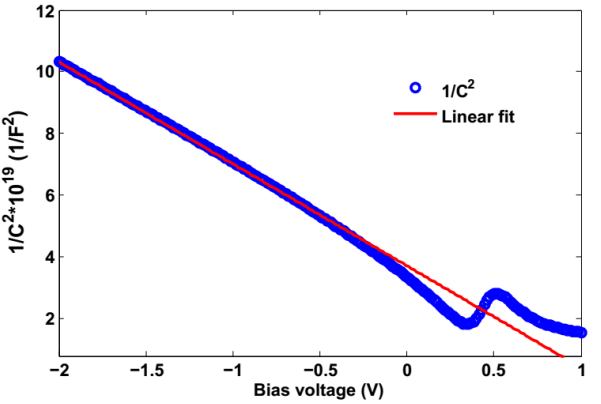

Fig.3. $1/C^2$-V plots of Fe/n-$Si_{0.85}Ge_{0.15}$ SBD.

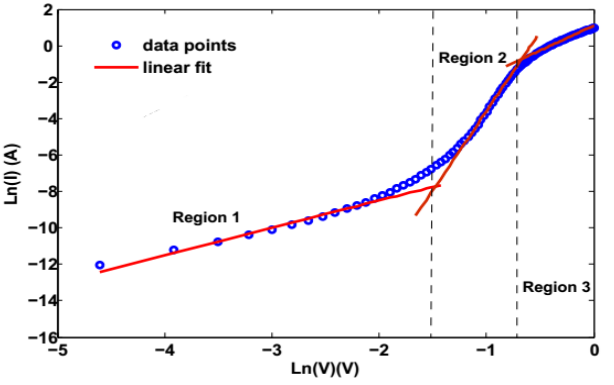

Fig.4. Forward ln(I)-ln(V) characteristics of Fe/n-$Si_{0.85}Ge_{0.15}$ SBD.

At high voltage forward bias, nonlinearity of *I–V* characteristics indicates a continuum of interface states in equilibrium in the semiconductor [22]. The interface state density is given by:

$$N_{SS}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_S}{W_D}\right] \qquad (8)$$

where W_D is space-charge region width, $n(V)=V/(kT/q)\ln(I/I_S)$, δ is thickness of interfacial insulator layer and ε_i and ε_S are permittivity of insulator layer and semiconductor, respectively. In n-type semiconductors, the energy of interface states E_{SS}, with respect to the bottom of the conduction band E_C, at semiconductor surface, is given as [23, 24, 22, 25]:

$$E_C - E_{SS} = q(\phi_e - V) \qquad (9)$$

For each bias voltage, values of interface states density N_{SS} in equilibrium with semiconductor are obtained from equation (8) by substituting voltage dependent $n(V)$, and taking δ = 85 Å, $\varepsilon_S = 12.9\varepsilon_0$ and $\varepsilon_i = 3.8\varepsilon_0$ [1]. Insulator layer thickness was calculated from C–V characteristics (not given here) using the equation $C_{ox} = \varepsilon_i\varepsilon_0 A/\delta$, where C_{ox} is the capacitance of interfacial layer.

Equations (8) and (9), along with I-V characteristics can be used to determine interface state density as a function of interface states energy E_{SS} with respect to the bottom of conduction band. N_{SS} was converted to a function of E_{SS} using equation (9) and is shown in Fig.5. Often, one observes an increase in diode effective barrier height ϕ_e in forward bias. This is due to the increase in quasi-Fermi energy level of majority carriers on semiconductor side. This causes most electrons to be be injected directly into the metal forming a thermionic emission current, though few of them are trapped by interface states. This charge capture process results in an increase in effective barrier height thereby reducing diode current [26, 27].

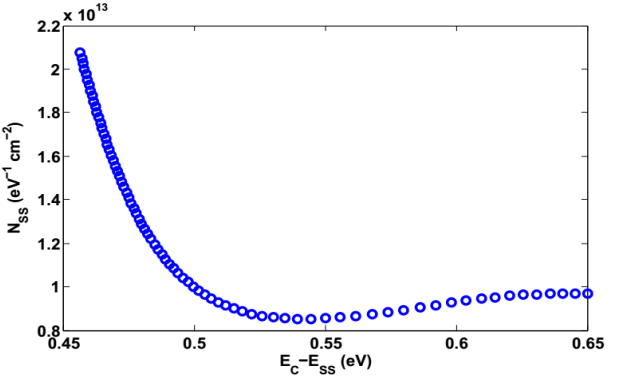

Fig.5 N_{SS} energy distribution profile for Fe/n-$Si_{0.85}Ge_{0.15}$ SBD.

Interface state density determined by Teman's method [28] is found to be 3.79 ×10^{12} $cm^{-2}eV^{-1}$. From Fig.5, it can be seen that an exponential increase in interface states density exists from mid gap towards the bottom of the conduction band.

4. Conclusion

In this study, electrical properties of Fe/n-$Si_{0.85}Ge_{0.15}$ Schottky contact have been characterized using current-voltage (I-V) characteristics at

room temperature. The observed non-ideal forward bias I-V behavior is attributed to a change in metal/semiconductor barrier height due to interface states, an interfacial layer and series resistance. The partial applied bias voltage drop across the interfacial layer causes a forward current drop that leads to a deviation from ideal I-V characteristics. Calculated ideality factor obtained from I-V characteristics is higher than unity and is attributed to the presence of an interfacial layer. Calculated barrier heights from I-V and C-V measurements show some discrepancy that is attributed to barrier height inhomogeneity at the Schottky interface. The downward curvature at sufficiently large voltages is caused by series resistance effect. R_S value has been calculated using Norde method. It is clear that ignoring the role of series resistance, interface state density and interfacial layer can lead to significant errors in electrical characteristics of devices.

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