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Study of interface trapped charges effect on performance of junction less trial material cylindrical surrounding-gate MOSFETs

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Abstract

Interface trapped charges effect on the performance of Junction Less-Trial Material Cylindrical Surrounding-gate MOSFETs (JLTMCSG-MOSFETs) has been studied. An analytical model has been used for this purpose, it is based on solving the two-dimensional Poisson's equation in cylindrical coordinates. The device performance has been investigated as a function of surface potential, electrical field, drain induced barrier lowering (DIBL), subthreshold Slope (SS) and threshold voltage (Vth). The obtained results show that the performance of the device was improved when using the trial material gate with different work functions and interface trapped charges. This study confirms that the analytical model used is useful not only for circuit simulations, but also for device design and optimization.

Keywords: Surrounding-gate MOSFET; Gate-Trial-material; Junctionless transistor; Trapped charges.

1. Introduction

The size of metal-oxide-semiconductor field-effect transistors (MOSFETs) has not stopped decreasing during the last years. The problem of the traditional MOSFETs is in the short channel effects (SCEs) [1, 2], that's why the cylindrical surrounding-gate (CSG-MOSFET) is considered as one of the most suitable solutioin for the problem. Indeed it extends the scaling limit to nano-MOS technology [3, 4], because of its ideal good gate control ability and symmetric structure. CSG MOSFETs provides the possibility to remove the SCEs for a given oxide thickness and channel length [5-7]. To overcome these challenges, a new type of device named junctionless (JL) transistor is recommended [8]. The doping concentration of the JL transistor is constant through the three regions: source, channel and drain [9-11]. The junctionless technology is known to have several benifits such as the disappearance of abrupt junctions, which is eliminated at the nanometer scale, using simpler fabrication process. Thus it is expected that the volume conduction implying that surface roughness scattering and flicker noise to be reduced [12]. Moreover, even for JL transistor, DIBL cannot be neglected, it is why a tri-material gate (TMG) structure has been used [13], in order to enhance the immunity against DIBL [10, 12].

The interface traps and the oxide charges act effectively on the device, they can modify the surface leakage current in the p-n junction, or modify their avalanche breakdown voltage, they can also lead to the appearance of undesirable current paths between the elements of an integrated circuit. At the Si-SiO2 interface, the traps are considered as defects, having energy levels within the band-gap of Si [14, 15]. The semiconductor / oxide interface can be simulated at equivalent localized interface charges [16, 17]. To carry out our study, we used an analytical model based on the precise resolution of the Poisson equation in two-dimensional cylindrical coordinates [13, 18]. The main purpose of this study is to see the impact of the trap charges on the performances of the device. The mathematical tool used is the superposition technique, where the Poisson equation is divided into two different equations; a two-dimensional homogeneous Laplace equation (2D) with its boundary conditions and a one-dimensional Poisson equation (1D), where the solution is obtained using the Fourier-Bessel series. Combining the advantages of the CSG structure, junctionless structure and tri-material gate structure, a new junctionless trial-material cylindrical surrounding-gate MOSFET (JLTMCSG-MOSFET) was suggested.

In addition, the effects of trapped charges on the flat band voltage were investigated, as well as the influence of the density and position of the localized interface charges (positive and negative) on the performance of (JLTMCSG-MOSFET) for different channel lengths were discussed as a function of the surface potential, the electric field, the lowering of the drain inducing barrier (DIBL), the subthreshold slope (SS), and the threshold voltage (Vth) at room temperature.

2. Device structure

Figure 1 shows the cross-sectional of a JLTMCSG MOSFET structure with localized interface charges, used for modeling and simulation. The JLTMCSG MOSFET consists in three gates, constituted by three different materials (M1, M2 and M3) having as work functions: $\Phi_{M1} = 4.8\ \text{eV}(\text{Gold}),\ \Phi_{M2} = 4.6\ \text{eV}\ (\text{Tungsten})$ and $\Phi_{M3} = 4.4\ \text{eV}\ (\text{Titanium})$. In addition the channel region can be splited into three parts with the same length (L1:L2:L3=1:1:1). Because of the cylindrical symmetry of the device structure, a cylindrical coordinate system is used, with r as radial direction and z as the horizontal one. The advantage of this type of structure is that it does not allow the variation of the potential and the electric field as a function of the angle in the plane of the radial direction, which means that the 2D analysis is sufficient. We consider also that the source/drain regions have no thickness and the source/drain contact is located along the left/right side of the heavily doped silicon channel. Added to these considerations, zero gate-to-S/D overlap is assumed. All calculations were done at room temperature.
The degradation of short channel MOSFET characteristics due to the interface trapped charges as one of the most important challenges to further progress of device doun-scaling. Recently interface trapped charges effect has been studied in cylindrical nanowire MOSFET [19], silicon nanowire pseudo-MOSFET [20] and DMG-S-SOI MOSFET [21].
Figure 2 shows the experimental device architecture with intrinsic trap states, where the charge trapping mechanism has been presented [22].

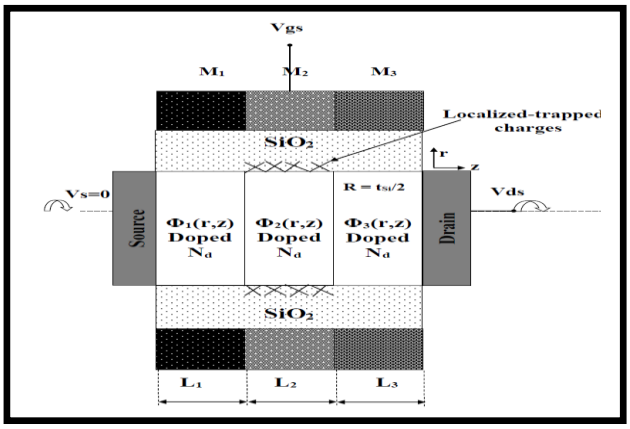

Figure 1. Cross-section view of JLTMCSG-MOSFETs.

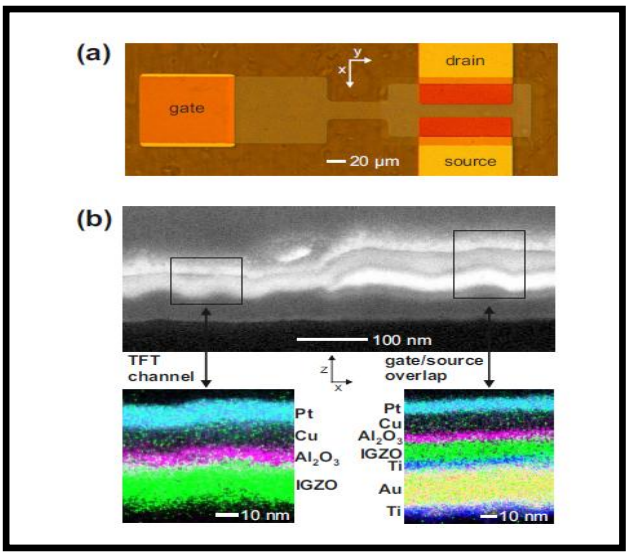

Figure 2. Experimentally realized thin-film transistor (TFT). (a) Optical micrograph of a thin-film transistor with a channel width of 100 μm and a channel length of 20 μm. (b) Cross section of a thin-film transistor (TFT)[22].

3. Analytical model

3.1. Electrostatic potential

By solving Poisson's equation in the three regions of the channel, the electrostatic potential can be written as follows [18]:

$$\frac{1\partial}{r\partial r}\left(r\frac{\partial}{\partial r}\phi_1(r,z)\right)+\frac{\partial^2}{\partial z^2}\phi_1(r,z)=\frac{qN_1}{\varepsilon_{si}},$$
$$0\le z\le L_1\ ,0\le r\le R,$$
$$\frac{1\partial}{r\partial r}\left(r\frac{\partial}{\partial r}\phi_2(r,z)\right)+\frac{\partial^2}{\partial z^2}\phi_2(r,z)=\frac{qN_2}{\varepsilon_{si}},$$
$$L_1\le z\le L_1+L_2\ ,0\le r\le R,$$
$$\frac{1\partial}{r\partial r}\left(r\frac{\partial}{\partial r}\phi_3(r,z)\right)+\frac{\partial^2}{\partial z^2}\phi_3(r,z)=\frac{qN_3}{\varepsilon_{si}},$$
$$L_1+L_2\le z\le L,\ 0\le r\le R, \qquad (1)$$

Using the superposition technique, the electrostatic potential in each region of the channel is written as follows [13, 18]:

$$\phi_j(r,z)=V_j(r,z)+W_j(r),\qquad j=1,2,3, \qquad (2)$$

Where: $W_j(r)$ and $V_j(r,z)$ are respectively the (1D) solution obtained from Poisson's equation and the (2D) solution of homogeneous Laplace equation, obtained considering boundary conditions.
The solutions of $W_j(r)$ is given by [18]:

$$W_j(r)=\frac{qN_j}{4\varepsilon_{si}}r^2+V_{gs}-\ /_{MS}-\frac{qN_j t_{ox}^2 R}{2\varepsilon_{ox}}-\frac{qN_j R^2}{4\varepsilon_{Si}},$$
$$j=1,2,3, \qquad (3)$$

Where: ϕ_{MSj} is the work function of different materials, given by [13]:

$$\phi_{MSj} = \phi_{Mj} - \phi_{Si} - V_{fb}\ , \quad (4)$$

ϕ_{Mj} being the metal work function, ϕ_{Si} the silicon work function, which can be written as:

$$\phi_{si} = \chi_{si} + \frac{E_g}{2q} + \phi_{Fh}\ , \quad (5)$$

Where: ϕ_{Fh} is the Fermi potential [18]:

$$\phi_{Fh} = \frac{kT}{q} ln \frac{N_h}{n_i}, \quad (6)$$

and:

$$V_{fb} = \frac{qN_f}{C_{ox}} \quad (7)$$

V_{fb} is the flat band voltage depending on the interface fixed charges N_f and the oxide capacitances C_{ox} [17].

Using the Fourier-Bessel series and separation method, the general solution $V_j(r,z)$ is expressed as:

$$V_j(r,z) = \sum_{n=1}^{\infty} \left[C_n^{(j)} exp\left(\frac{\alpha_n z}{R}\right) + D_n^{(j)} exp\left(\frac{-\alpha_n z}{R}\right)\right] J_0\left(\frac{\alpha_n r}{R}\right), \quad j = 1,2,3, \quad (8)$$

Where: α_n is the eigenvalue which satisfies the equation [18]:

$$\frac{\varepsilon_{ox} R}{t'_{ox} \varepsilon_{si}} J_0(\alpha_n) - J_1(\alpha_n)\alpha_n = 0, \quad (9)$$

$J_{i(x)}$: is the first term of the Bessel function of order i.

The Fourier-Bessel series coefficients $C_n^{(j)}$ and $D_n^{(j)}$ are obtained by applying boundary conditions [18].

2.3. Subthreshold current calculation

The current density (both drift and diffusion) can then, be written as [13, 23]:

$$J(r,z) = -q\mu_n n(r,z) \frac{d\phi_n(z)}{dz}, \quad (10)$$

Where: $n(r,z)$ is the carrier concentration and μ_n the electron mobility.

By integrating the current density $J(r,z)$ two times and through the z direction, we obtain:

$$I_{ds}(z) = \frac{2\pi N_D \mu_n KT\left[1-exp\left(-qV_{ds}/KT\right)\right]}{\int_0^L \left[\int_0^R r exp\left\{q[\phi(r,z)]/KT\right\} dr\right]^{-1} dz}. \quad (11)$$

3.3. Threshold Voltage Vth

The threshold voltage is defined as the gate voltage that causes the minimum surface potential to become two times the Fermi potential, i.e.,

$$\phi_1(r = R, Z = Z_{min}) = 2\sqrt{C_1^{(1)} D_1^{(1)}} J_0(\alpha_1) + V_{gs} - \phi_{MS} - \frac{qN_2 t'_{ox} R}{2\varepsilon_{OX}} \quad (12)$$

$$\phi_1(r = R, Z = Z_{min}) = 2\phi_F$$
$$V_{gs} = V_{th} \quad (13)$$

Where:

$$z_{min} = \frac{R}{2\alpha_1} \ln \frac{D_1^{(1)}}{C_1^{(1)}} \quad (14)$$

z_{min} is the minimum surface potential lies in region 1.

The threshold voltage can be obtained as:

$$V_{th} = \phi_{MS1} - U_t - \frac{(qN_1 R)}{2C_{ox}} - \frac{(qN_1 R^2)}{4\varepsilon_{si}} - 2\sqrt{Cn_1^1 Dn_1^1} \quad (15)$$

Where:

$$U_t = \frac{K_B T}{q} \quad (16)$$

4. Results

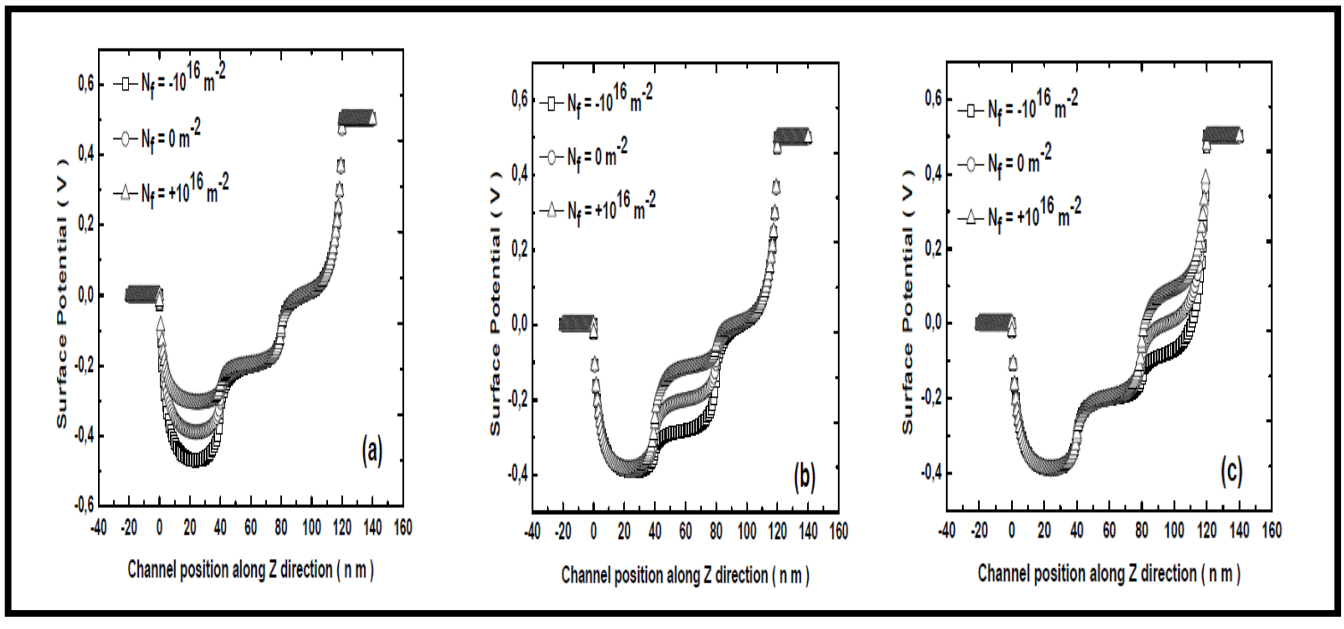

Figure 2. Surface Potential profile for JLTMCSG-MOSFETs with different trap charges density located near: a) Source, b) Center, c) Drain.

Figure 2 shows the surface potential profile with localized charges: near the source side, near the center and near the drain side. For positive (negative) localized interface charges, the surface potential is higher (lower) in the damaged region because the flat band voltage (V_{fb}) in the damaged region decreases (increases) depending on the nature of localized charges. The minimum surface potential appears in the damaged region, in the case of the negative charge density.

Figure 3 plots the variation of the electric field as a function of the channel positions with trap charges density as parameter. Two peaks of electric field appear wherever the trap charges are located, which means that we have a better electric field in the channel, which gives more acceleration to the electrons and improves the transport of the carriers in the channel. These peaks of electric field is mainly due to the structure of JLTMCSG-MOSFETs which has different materials i,e. different work functions.

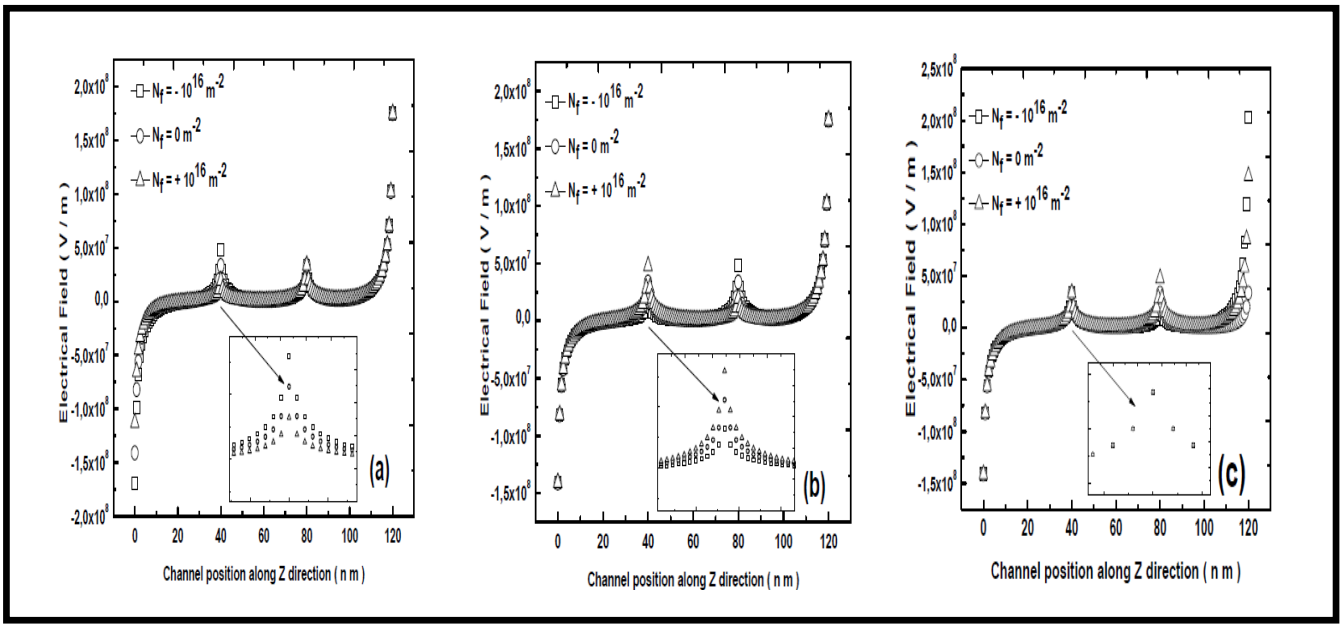

Figure 3. Electrical field versus the channel distance for JLTMCSG- MOSFETs with different trap charges located near: a) Source, b) Center, c) Drain.

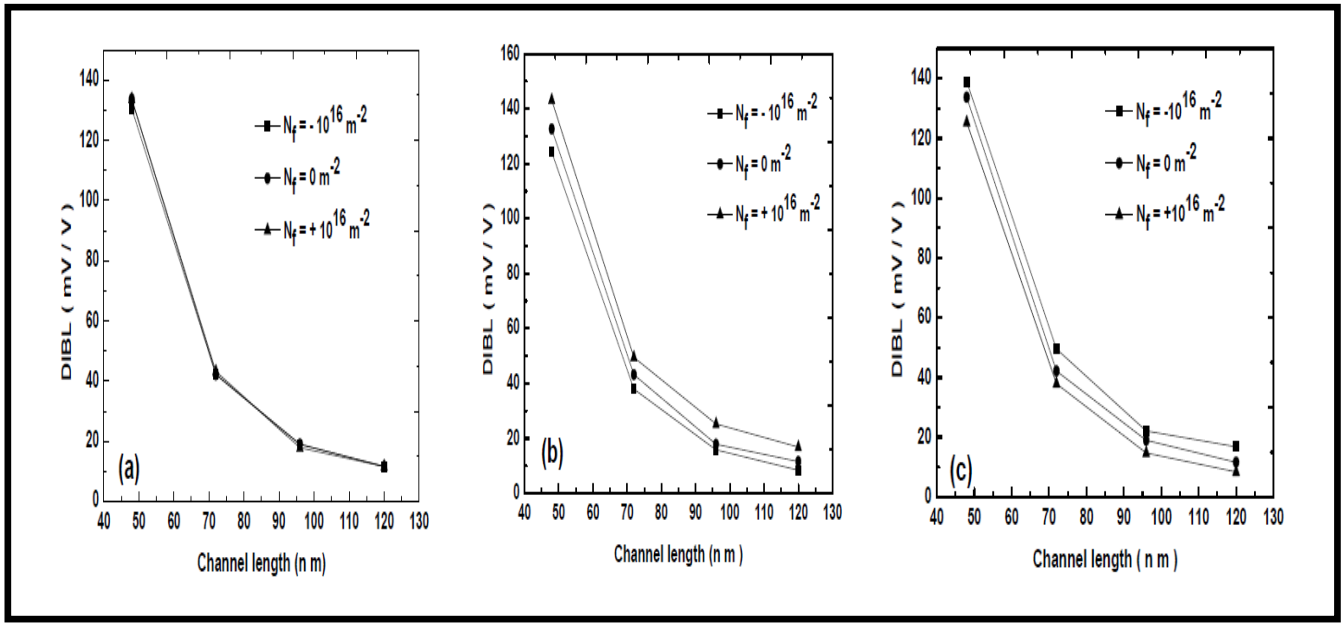

Figure 4. Drin-Induced Barrier Lowering (DIBL) variation with channel length for different trap charges density located near: a) Source, b) Center, c) Drain.

The DIBL is the short-channel effect in JLTMCSG-MOSFETs, it is attributed to the reduction of the threshold voltage of the device under high drain bias. In JLTMCSG-MOSFETs, the DIBL effect is still a new problem and requires further study, it is deduced using the following equation [24]:

$$DIBL = \frac{\Delta V_{th}}{\Delta V_{DS}} = \frac{V_{th\,1} - V_{th\,2}}{V_{DS\,1} - V_{DS\,2}} \quad (17)$$

In figure 4 we have represented the variation of the DIBL as a function of channel length for different localized trap charges (undamaged and damaged device), we remarked that the DIBL decreases when the channel length increases. For short channel length the influence of trap charges densities is insignificant in the case of the damage region localized near the source, otherwise we have a change in the DIBL when the trapped charge are located near the drain and in the center of the device. A low DIBL value (around 8 mV /decade) is observed in the case of a long channel, when the trap charges are located in the middle and near the drain of the device. We notice that, the DIBL is more sensitive to the channel length where effect of the drain voltage appear in short channel device, on the other hand, it is these affected to the trapped charges.

The subthreshold slope (SS) is a parameter to suppress the subthreshold characteristics of short-channel MOSFET devices in nanoscale range. A small sub-threshold slope is required for low threshold voltage and low power operation for small scale TECs.

The slope of the subthreshold is defined as the variation of the gate voltage corresponding to the change of a decade of the drain current, it is written as follows [24]:

$$SS = \Delta Vgs/\Delta(LogI_{DS}). \quad (18)$$

A theoretical subthreshold slope is around (60 mV/decade) at room temperature [25].

Figure 5 shows the variation of the subthreshold slope as a function of the channel length, it indicates that this one decreases when channel length increases, and it is higher (lower) in the case of positive (negative) localized charges densities. For the entire length of the gate, we can notice that the SS shift is about 4% when the localized charges change sign, from the minus sign to the plus sign. Moreover we have calculated the SS for localized charges near the drain and in the center of the device, the same results are obtained. This confirms that the subthreshold slope is independent of the position of trap charges. These variation is related to enhancement in the subthreshold current (i,e.).

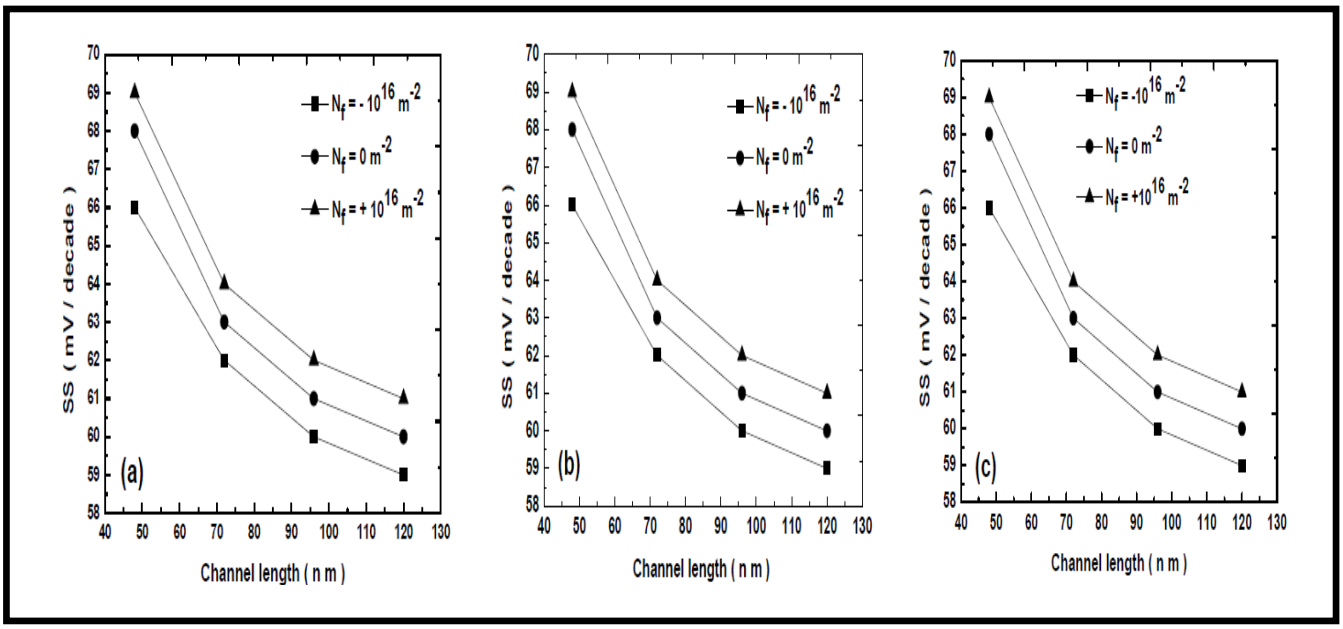

Figure 5. Subthreshold slope (SS) variation with channel length for different trap charges density located near: a) Source, b) Center, c) Drain.

Figure 6 shows the threshold voltage Vth variation (with and without trap charges) as a function of the channel length: the increase in the channel length leads to an increase in the threshold voltage, which improves the gate control in the channel region. In addition, we have studied the trap charges densities effects on JLTMCSG-MOSFETs. In the case of the trap charges localized near the source region (Fig. 6.a), the effect of the trap charges interface is significant. Higher values of Vth are obtained for negative sign trap charges. On the other hand, when the trap charges are localized in the center of the channel (Fig.6.b), the effect of these later is smaller. However in the case of trap charges localized near the drain region (Fig. 6.c), we record a negligible effect.

The rate of change in threshold voltage because the minimum of surface potential is changed with density of localised charges and its position.

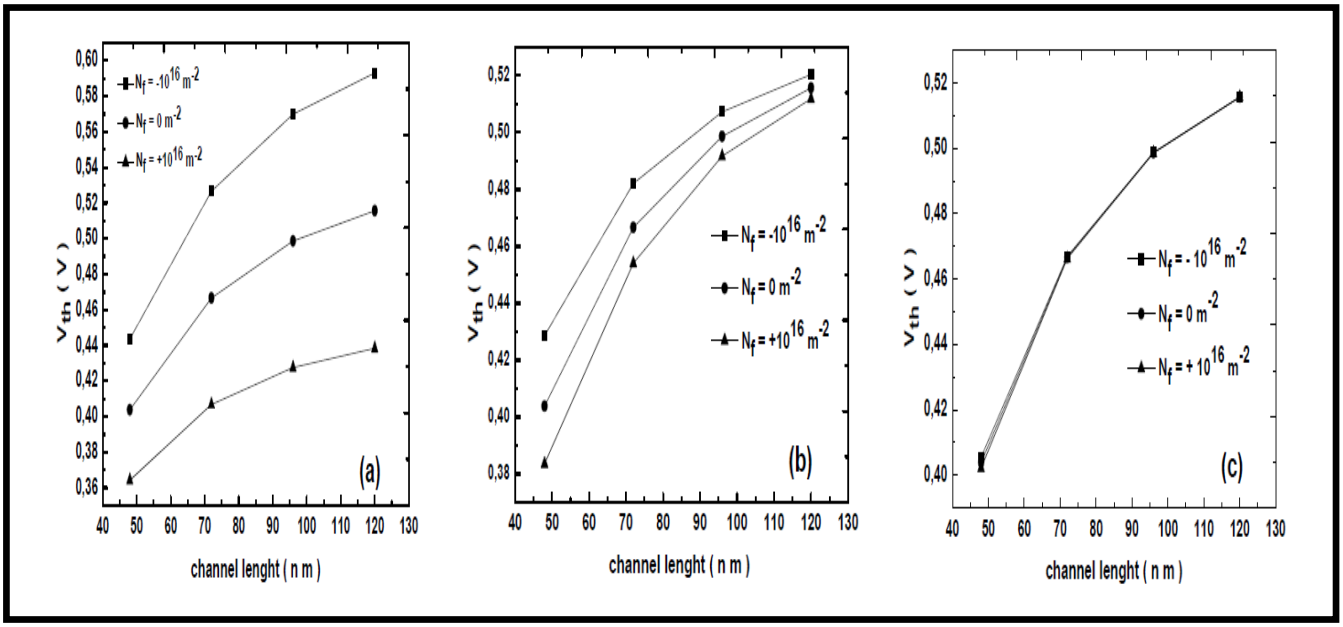

Figure 6. Threshold Voltage (Vth) variation with channel length for different trap charges density located near: a) Source, b) Center, c) Drain.

5. Conclusion

The impact of the density and localized interface traps charges on the electrical performance of the junction less Tri-material cylindrical surrounding-gate (JLTMCSG-MOSFET) has been studied, using analytical model, based on solving of the two-dimensional Poisson's equation in cylindrical coordinates. It has been observed that the presence of localized charges at Si–SiO2 interface causes a shift in the potential profile. For the electrical field, we have observed two peaks wherever the trap charges are located. The results show also that the effect of the localized interface trapped charges on drain-induced barrier lowering (DIBL) and on the subthreshold slope is slight for different channel lengths. However, its effect on the threshold voltage becomes more significant when the trapped charges are localized near the source region.

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