Journal of New Technology and Materials
JNTM
Vol. 05, N°01 (2015)32-35

OEB Univ. Publish. Co.

A study of C(V) characteristics of capacitors containing high-k oxides and high mobility carriers semi-conductors.

Amina Merzougui, Saida.Latreche and Seloua Bouchekouf

Dpt. Electronique, Fac. Sciences and technologies, Constantine university (25000), Algeria.

Received date: April 14, 2015; revised date: May 25, 2015; accepted date: May 29, 2015

Abstract

In this work, we proceeded to the analysis of C(V) characteristics of MOS capacitors (Metal-oxide-semi-conductor) with metal gates.

Within the framework of the search for new materials, we have studied C(V) characteristics of structures containing high permittivity oxide (high-k)- the HfO_2 in our case- to replace the ultra-thin conventional oxide layer (SiO_2) which reaches its physical and technological limits (less than 1 nm thickness).

In these same structures, the stacking of grid is deposited on a substrate with high mobility carriers (electrons and holes). In fact: The germanium (Ge) and III-V materials [1].

The obtained results were largely compared with others simulated and experimental ones.

Keywords: MOS capacitors, C(V) characteristics, High permitivity, high mobility carriers, Schrodinger.

1. Introduction

The micro-electronics industry succeeded in developing the MOSFET transistor as well as the circuits which integrate it, this is in order to satisfy society requirements.

This spectacular developpement is essentially caused by the concept of the miniaturization based on the reduction of all component's dimensions, particularly, channel's length and oxide's thicknesses.

However, this reduction is never without fatal consequences on the behavior of these miniature components.

In fact, several parasitic effects take place and degrade clearly the component's behavior, especially, leakage currants through the oxide layer [1, 2, 3].

For this reason, new alternatives are explored in the framework of the search for new materials and new architectures, used to cure these problems, and then, to improve components performances.

In this context, this present work shows the famous performances of the basic structure of all MOS technology components. In fact: The MOS capacity, having the double-layred (HfO_2 / SiO_2) as a grid oxide, which is deposited on a substrate with high mobility carriers semi-conductors [1, 4].

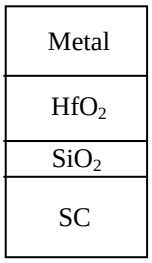

Fig.1: *Presentation of the studied structure containing High-k oxide*

For that, we proceeded to obtaining C(V) characteristics of the MOS structure described above, and this, by resolving the coupled « Poisson » and « Schrodinger » equations, this resolution was done numericaly, using Newton-Raphsson iterative method [3].

2. The role of the High-k gate oxide in new structures:

The principle is then to replace the ultra thin layer of (SiO_2) conventional oxide, by another thick layer of high-k oxide. Theses capacities are electrically equivalent, but the structure containing high-k oxide

constitutes a good remedy to leakage currents problems. In real structures, oxide layer results from the native oxidation of the substrate surface during its deposit. The following figure is more explanatory [5]:

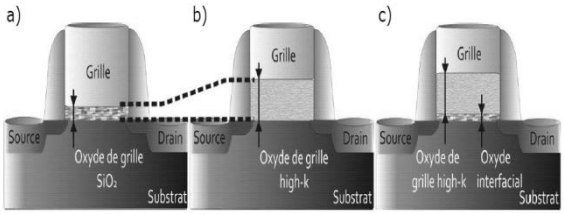

Fig.2: (a) : Conventional oxide . (b) : Integration of High-k oxide. (c) : Real structure

In this case, we can't speak of oxide thickness, but rather, of the equivalent oxide thickness EOT (Equivalent Oxide Thickness) given by the following expression [1, 5]:

$$EOT = t_{SiO2} = (\varepsilon_{SiO2} / \varepsilon_{High\text{-}k})\ t_{High\text{-}k}$$

Then, with a larger physical high-k oxide thickness, and equivalent electrical characteristics, the leakage current is strongly reduced involving an increase of the ratio I_{ON}/I_{OFF}, which is so beneficial for MOSFET transistors.

3. Equations and numerical details:

Obtaining C(V) characteristics requires then the self-consistent resolution of the following system [3] :

$$\begin{cases} \dfrac{d}{dx}\left(\varepsilon_0\ \varepsilon_{si}\ \dfrac{d}{dx}\right)\phi(x) = -q\left[p(x) - n(x) - N_A^-(x)\right] \\ -\dfrac{\hbar^2}{2}\dfrac{d}{dx}\left(\dfrac{1}{m^*}\dfrac{d}{dx}\psi_i(x)\right) + V(x)\ \psi_i(x) = E_i\ \psi_i(x) \end{cases}$$

Where ε_{si} is (Si) dielectric constant , Φ (x) is the electrostatic potential, $N_A^-(x)$ is ionized acceptors concentration, n(x) and p(x) are respectively free electrons and holes concentrations, ħ is the reduced Plank constant, m^* is electron effective mass, E_i et ψ_i are respectively, the confinement energies in the quantum well and equivalent wave functions . (x) is the spatial coordinate.

We point out that « Schrodinger » equation allows to model quantum phenomena which appear under the oxide – at the interface (ox/sc) -. Indeed, the small thickness of used oxides and the high doping levels, cause a strong electric field at the substrate surface, which makes curve the energy bands (conduction and valence) at the surface [6]. A quantum well is then created, carriers are confined into and are assimilated to a two-dimensional gas, their movement is free in the plan of the structure but confined in the perpendicular one [2, 5].

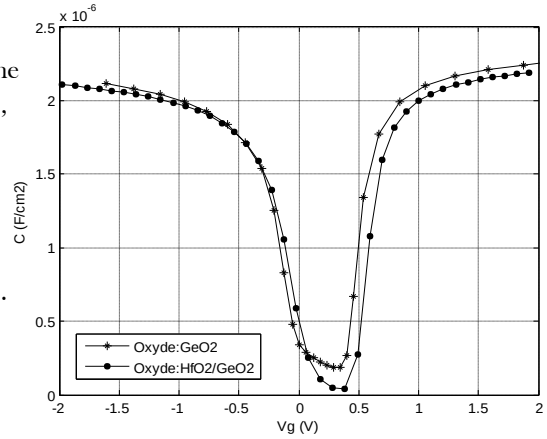

Fig.3: One layer oxide GeO_2. Bi-layer oxide HfO_2/GeO_2

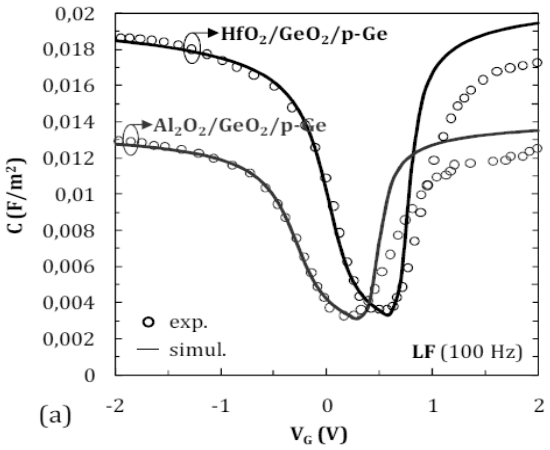

Fig.4: Structure with bi-layer oxide: HfO_2/GeO_2 [1,4]

4. Modeling of C(V) characteristics :

The resolution of the coupled system presented below, provides us carrier concentrations (electrons and holes) and also, the electrostatic potential in each mesh point of the structure, and this, for each applied oxide bias.

The total potential applied to the gate (V_g) is then calculated via the following expression [7]:

$$V_g = V_{ox} + V_{FB}$$

Where V_{FB} is the flat band potential [5] :

$$V_{FB} = \Phi_M - (\chi + Eg/2 + Efs)$$

- Φ_M is the work function of the metal gate.
- χ, Eg and Efs are respectively the electronic affinity, the bandgap and

the Fermi energy of the semi-conductor.

The capacitance is then obtained by differentiating the total charge in the substrate and the gate bias according to the expression [3]:

$$C = \Delta Q / \Delta V_g$$

5. Results

5.1. Interest of high permittivity oxides :

We simulated the C(V) characteristics of a capacitor with a bi-layer oxide (t_{HfO2} = 4 nm et t_{SiO2} = 1.4 nm), which corresponds to an equivalent oxide thickness of EOT=2.3 nm approximately. This stacking being deposited on a (Ge) substrate doped (P) at $10^{17}cm^{-3}$, the gate metal having a work function of 4.6 ev.

The (Fig.3) represents C(V) characteristics of the two structures presented bellow, it shows clearly that they are electrically equivalent. That containing High-k stacking, has in additional, the advantage of decreasing leakage currents because of its physical thickness relatively large.

Our C(V) are very comparable with those simulated by [1,5].

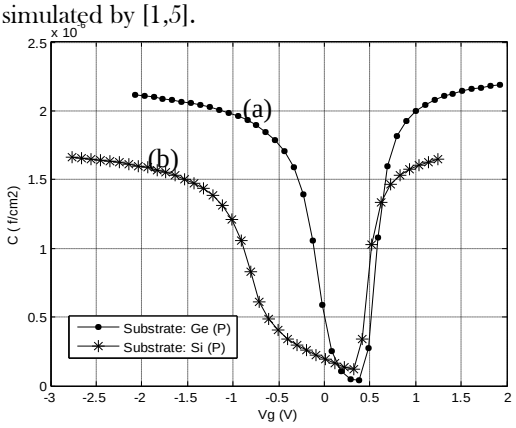

Fig.5: Bi-layer HfO_2/GeO_2 (a). Bi-layer HfO_2/SiO_2 (b)

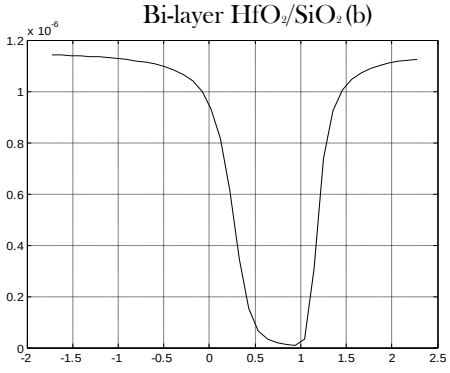

Fig.6: C(V) curves of a structure with GaSb substrate

5.2. Influence of substrate with high mobility carrier:

- *Germanium (Ge) substrate:*

We simulated in this time, the C(V) characteristics of two different capacities : the first one having the bi-layer oxide (HfO_2/GeO_2) deposited on a Ge(P) substrate, while the second one is constituted of the bi-layer oxide (HfO_2/SiO_2) deposited on a Si(P) substrate.

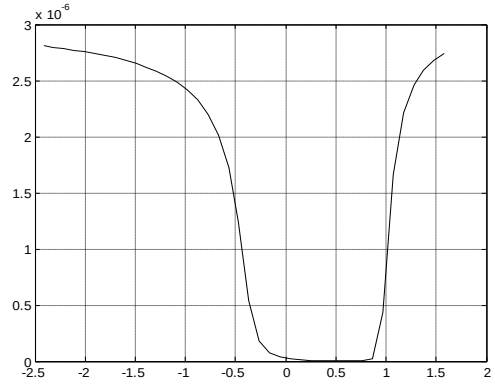

Fig.7 : C(V) curves of a structure with GaAs substrate

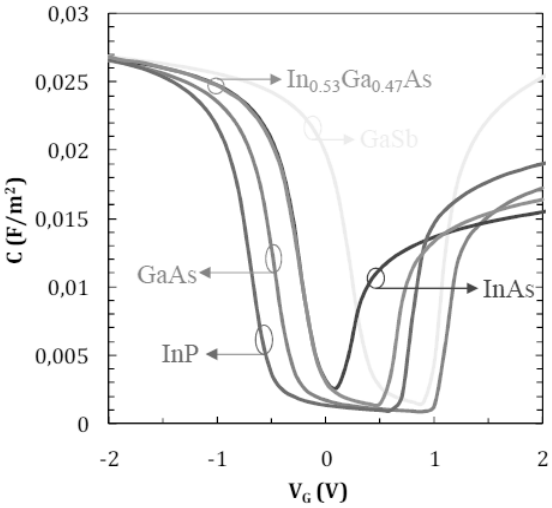

Fig.8 : C(V) Curves with substrates in different III-V materials simulated by [1]

The introduction of High-k oxides in new structures is always accompanied by an interface states density, which tends to trap free carriers and then, to decrease the drain current in transistors. For this reason, a radical change of the substrate material was considered. Indeed, materials with high mobility carriers cure rather well trapping problems.

In the other part, Germanium (Ge) with its small bandgap with respect to that of Silicon (Si), ensures a short depletion region in term of gate voltage. The passage from the accumulation to the

inversion mode, is then so rapid, this is clearly shown on the (Fig.5).

- *Substrate in (III-V) materials :*

(Fig.6) and (Fig.7) represent C(V) curves obtained for structures containing (III-V) materials, respectively : The (GaSb) and the (GaAs), they confirm in their turn that the speed of the passage from accumulation to inversion mode is directly related to the smallest bandgap ($E_{g\,(GaSb)} < E_{g\,(GaAs)}$).

These results are also in a good agreement with those obtained by [1] (Fig.8).

6. Conclusion

In this paper, we presented a work which permits us to highlight the interest of high permittivity oxides integration in new generations of MOSFET transistors.

Indeed, these High-k oxides permit obtaining the same electrical properties of capacitors containing ultra-thin oxides, but by using physical thicknesses relatively large. This will largely cure leakage currents, which exceed 1A/cm^2 for t_{SiO2} thickness of about 1nm.

Also, using substrates containing high mobility carriers is a good solution to counter the effect of carriers trapping by the interface states appearing during the integration of high-k oxides.

The obtained results show clearly the substrate band gap effect on the depletion region, this effect describe the commutation from accumulation to inversion mode and decides then of transistors drain current.

Our simulated results are in a very good agreement with other simulated and experimental ones obtained by other authors.

This permits us to validate our simulation code and proves its efficacy.

Réferences

[1] M. Moreau, « *Modélisation et simulation numérique des nano-transistors multi-grilles à matériaux innovants* ». Thèse de doctorat, Université de Provence, Marseille, France, 2010.

[2] E. Jordana, « *Conception, réalisation et caractérisation de grilles en Silicium polycristallin déposé amorphe à basse température et dopé Bore in situ* ». Thèse de doctorat, Université Paul Sabatier, Toulouse, France, 2005.

[3] A. Merzougui, « *Etude des courants de fuites de type SILC dans les cellules EEPROM* ». Thèse de doctorat, Université Mentouri, Constantine 1, Algérie, 2010.

[4] M. Moreau a,*, D. Munteanu a, J.-L. Autran a,b, F. Bellenger c, J. Mitard c, M. Houssa c, « *Investigation of capacitance–voltage characteristics in Ge /high-j MOS devices», Journal of Non-Cristalline Solids,* Vol. 355, pp. 1171 - 1175, 2009.

[5] T. Nguyen, « *Caractérisation, modélisation et fiabilité des diélectriques de grille à base de HfO2 pour les futures technologies CMOS*». Thèse de doctorat, INSA, Lyon, France, 2009.

[6] B. Diagne, « *Etude et modélisation compacte d'un trasistor MOS SOI double-grille dédié à la concéption* ». Thèse de doctorat, Université Louis Pasteur, Strasbourg I, France, 2007.

[7] C. Plossu, « *Caractérisation et fiabilité des oxydes minces SiO_2 dans les dispositifs MOS* ». Habilitation à diriger des recherches, Université Claude Bernard, Lyon I, France, 2000.

[8] A. Delabie, F. Bellenger, M. Houssa , T. Conard, V. Elshocht, M. Caymax, M. Heyns, M. Meuris « *Effective electrical passivation of Ge (100 for high-k gate dielectric layer using germanium oxide)», Appl.Phys. Lett,* Vol. 91, N°:8, pp. O82904, 2007.