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Temperature variation effects in partially depleted SOI n-channel MOSFETs

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Abstract:
Silicon-on insulator (SOI) technology has attracted a great attention as a probable alternative candidate for low power, high performances applications. Nowadays electronic is subjected to temperature variations and is, some time, obliged to operate at high temperature. In this paper, based on some simulations results we obtained using ATLAS SILVACO TCAD software, we have investigate the impact of temperature variation on the electrical properties of a PD SOI n-MOSFET. This study allows us to highlight the existence of a ZTC point as well in the linear that in the saturated region. We also examine the off state leakage current dependence with temperature. At the end of this workself heating effects are also studied.
Keywords: Temperature effects; SOI MOSFETS, ZTC point, self heating effects, leackage current.

1. Introduction

Electronic is continually and always subjected to temperature variations, and is consequently constraint to operate at different temperatures. The typical examples are that of the automobile, the military, the space, and the nuclear industries. In these industries integrated circuits "ICs" used are often constrained to operate at very high temperatures much beyond 150 ° C. Knowing that semiconductors are very sensitive to temperature variations,it becomes crucial to understand the phenomena caused by these variations and their implications. These implications do not occur only on physical quantities but also on the electrical ones of designed devices conceived for applications where temperature variation or high temperature applications are expected. The operating temperature of components and consequently of circuits has a direct influence on their electric characteristics. A high operating temperature leads undeniably to their ageing. Temperature variations deteriorate ineluctably the correct operation of analog and digital ICs in terms of power dissipated in stand-by mode, speed, and accuracy. As a result, various technologies have been investigated as being a probable alternative intended for operations particularly at high temperatures. These explored technologies comprise GaAs [1], CMOS [2] and SOI [3] technologies. At high temperature, CMOS technology is unfortunately restricted in its operation by the existence of latch up phenomenon inherent in this technology, and by the presence of high leakage current through its well junction. Hence, other materials, such as III-V, SiC or diamond, have the ability to operate above 500 ° Celsius, but have unfortunately not the necessary maturity to be exploited to short or even medium term. While GaAs seems much more favorable than silicon for high temperatures application, it remains largely supplanted by SOI-CMOS technology in terms of stability with respect to temperature fluctuations. Indeed, the use of SOI- CMOS devices seems to be an excellent alternative to operate at high temperature, this is of course essentially due to the absence of latch-up phenomena with a sufficient reduction of leakage current

In this paper, we will investigate the temperature variation effect on the I_{DS}–V_{GS}, I_{DS}–V_{DS} and gm–V_{GS} characteristics , we will also investigate the zero temperature coefficients biasing point called "ZTC" of SOI MOSFETs using ATLAS SILVACO software. We will also examine the impact of temperature variation effect on the off state current of our device. At the term of this workself heating effects are also presented.

2. Overview of SOI technology

In the 1960's the necessity for radiation hard devices in the military and space industry had lead to the development of silicon on-insulator devices. During 1970s and '80s some SOI materials and structures were designed for dielectrically separating the thin active device volume from the silicon substrate.

SOI technology has several industrial processes that have been developed in order to make a Silicon film on an insulating layer called buried oxide "BOX". The oldest process is the Silicon-On-Sapphire called "SOS" and also called hetero-epitaxy process, in view of the fact that silicon and sapphire are different materials with different crystallographic structures. SOS substrates are obtained by growing a thin silicon film on the top of a monocristalline sapphire substrate. Since the 1980s, other techniques have been developed and have become industry standards. The two main processes are Separation by Implantation of

Oxygen called SIMOX and Bounded SOI Wafer called BSOI [4], [5]. In SIMOX process, considered as the dominant technology this last decade, oxygen ions are implanted below the surface of a bulk Si wafer, after that, a thermal annealing allows creating a SiO2 layer buried inside this wafer. In BSOI process, wafer bonding materials can be obtained by gluing two wafers togetherand creating hydrogen bonds between these two wafers.Primary, a bulk silicon wafer (wafer A) is oxidized then, a high-energy implant of hydrogen ions is carried out in order to generate defects at a fixed depth in this wafer, by using hydrophilic bonding, it is then bonded to a second silicon bulk wafer (wafer B). After a thermal annealing, the wafer A is divided into two parts, a small monocristalline silicon which remains bonded to the wafer B, and the rest of the wafer A [6],[7]. SIMOX and BSOI are considered as being the main processes [4], [5].; with a technique derived: the Smart Cut technology. This technique currently dominates the SOI market, and represents about 90% of actual SOI production [8].

SOI MOSFETs that are built on a thin silicon layer situated on the top of an insulator layerprovides a robust vertical isolation from the substrate and reduces dramatically the junction capacitance [9],thus doing this device much faster than a standard silicon-based device. If the thin silicon film, used to build active devices and circuits, is thin enough the depletion zone below the gate extends all the way through the BOX, and the device shown in Figure 1.A is called fully depleted, if not, and generally if the silicon film is currently thicker than 100 nm as shown in Figure 1.B it is called partially depleted. The much important characteristic of FD SOI MOSFET is that the current drive is higher than in bulk MOSFET and its subthreshold slope is sharper due to an much smaller body factor [10].

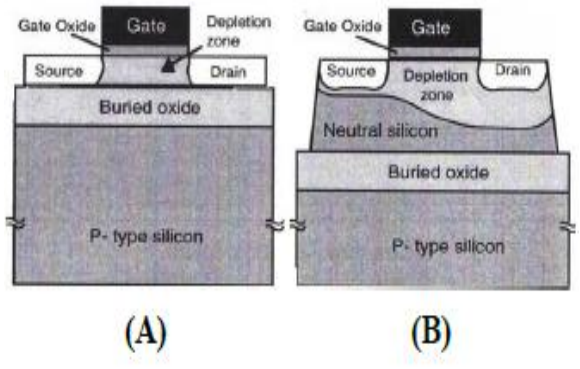

Figure 1. (A) - Fully depleted SOI MOSFET. (B) -Partially depleted SOI MOSFET [11].

Generally, SOI MOSFETs owning a thin SOI layer (usually lower than 50 nm) with all body areas under the channel depleted are called fully depleted SOI MOSFETs (FD-SOI). Conversely, SOI MOSFETs, owning a thick SOI layer (usually greater than 100 nm), with some areas at the bottom of the body area that are not depleted, are called partially depleted SOI MOSFETs (PD-SOI).

3. SOI MOSFETs operation according to depletion zones Thickness

Silicon active layer thickness, t_{si}, is the most important parameter in the classification and operation of SOI MOSFETs. According to this thickness, localized between the BOX and gate oxide, SOI MOSFETs operation and various physical phenomena in these components change [8].

In SOI devices, both of the gate/oxide gate/ body and substrate/ buried oxide/body form a metal-insulator-semiconductor structure. As a result two depletion zones are present in the active region. The first region is controlled by the top gate when the second region is controlled by the substrate that is considered as a back gate. Each gate requires a surface potential for its Si/SiO2 interface and an operating regime: accumulation, desertion, inversion. When the metal-insulator-semiconductor structure operates under strong inversion the depletion zone thickness is maximum and equal to X_{dmax}. In this case, the surface potential is nearly equal to $2\Phi_F$. Under these conditions the maximum depletion width X_{dmax}, for a PD MOSFET of each depletion zone can be expressed by [12]:

$$X_{dmax} = \sqrt{\frac{4.\varepsilon_{si}.\emptyset_F}{q.N_A}} \qquad (1)$$

$$\emptyset_F = \frac{k.T}{q}.\ln\left(\frac{N_A}{n_i}\right) \qquad (2)$$

Where $\varepsilon_{si}$is the relative dielectric permittivity of silicon(F/m) , N_A the Silicon layer doping (cm^{-3}), Φ_F the Fermi potential(V), n_i the intrinsic electron density (cm^3), K Boltzmann's constant (eV/°K), q the Electron charge(cb) and T the temperature (°K).

The depletion conditions according to depletion zone thickness Xdmaxare summarized in table 1.

TABLE I
SOI MOSFET Operation according to depletion zones thickness.

	$T_{si}<X_{DMAX.}$	$X_{dmax}<t_{si}<2_{max}$	$t_{si}>2\ X_{dmax}$
Silicon film	Fully Depleted mode	Not Fully Depleted .Depend on bias conditions.	Partially-Depleted-mode.

According to biasing conditions and doping conditions, the two depletion zones cover partially or totally the silicon film of the active zone.

4. Temperature parameters sensitivity of the PD SOI n-MOSFETs.

The PD SOI n-MOSFETS may be considered because of the neutral region in the fin film, as an association of a MOSFET transistor located in the top portion of thin film and a parasitic BJT located in the bottom portion of this thin film. The device temperature-dependent parameters, mentioned briefly in the following, include electron mobility, intrinsic concentration, impact ionization coefficients and generation/recombination lifetimes.

4.1. Influence of temperature on electron mobility

In the Philips unified mobility model, there are two contributions to carrier motilities. The first contribution represents phonon (lattice) scattering and the second one takes into account all other bulk scattering mechanisms due to free carriers, and ionized donors and acceptors. This electron mobility μ_{eff} depends on the doping density, and on the operating temperature. This temperature dependence can be expressed as [13]:

$$\mu_{eff} = g_s\left(\frac{1}{\mu_{lattice}} + \frac{1}{\mu_{impurity}}\right) \quad (3)$$

$$\mu_{eff} = g_s.\left(\frac{1}{\mu_{l0}\left(\frac{T}{300}\right)^{-2.2}} + \frac{1}{\frac{A.T^{1.5}}{N_A}\left[ln\left(1+\frac{BT^2}{N_A}\right)-\frac{BT^2}{BT^2+N_A}\right]}\right)^{-1} \quad (4)$$

Where g_s is represents the surface reduction factor due to the surface scattering effect and is equal to 0.5, A and B parameters depends on the doping density N_A, A and B are equal to $A=3,5.10^{1}(cmVS)^{-1}$,$B=1,52.10^{15}\ cm^{-3}K^{-2}$[13].

4.2. Influence of temperature on intrinsic concentration

Temperature dependant intrinsic concentration n_i is expressed as:

$$n_i(t) = \sqrt{N_c N_v}.exp\left(-\frac{E_g}{2kT}\right)$$

$$= \left[\frac{2\pi k\left(m_n^* m_p^*\right)^{0.5}}{h^2}\right]^{\frac{3}{2}} T^{\frac{3}{2}} exp\left(-\frac{E_g}{2kT}\right) \quad (5)$$

Where m_n^* and m_p^* are the electron and hole effective mass respectively, Eg is the silicon band gap (eV), h Planck's constant (Js) and k the Boltzmann's constant.

When the operating temperature increases silicon bandgap narrows, $n_i$increases, the related Fermi-potential and the depletion width in the device can also change.

4.3. Generation/Recombination lifetime

As cited above, the PD SOI n-MOSFET may be considered, as an association of a MOSFET transistor located in the top portion of thin film and a parasitic BJT located in the bottom portion of this thin film. For BJT transistors electron lifetime in the neutral region, generation lifetime and the recombination lifetime in the depletion region increases when the temperature increases affecting the leakage current of the device which increases as well.

The impact of the temperature variation on the cited parameters leads to drain current, threshold voltage and kink effect variation.

5. Results

Numerical simulation is an extremely helpful tool for detailed investigation of physical phenomena .It allows to determine the electrical characteristics of semiconductor devices. Technology Computer Aided Design (TCAD) is the most universally used simulation tools. Simulation results presented in this study had been performed using Atlas SILVACO Software [14].Thisdevice simulator offer many physical variables.

The main device parameters that influence the electrical behavior of our device are: its doping profile in and near the channel regions, the oxide "ε_{ox}" dielectric constant, oxide thickness "t_{ox}", the electrical gate length and gate work function, channel doping, source and drain doping, gate length L_G, length of source and drain junction . Actually, device simulator offers more variables, such as those used by physical models like mobility models simulator that influence strongly the electrical behavior of the device. The investigations provided in this work were carried out for an SOI n-MOS transistor; their extension to a P channel MOSFET device is straightforward. The starting point for our simulations is a basic structure represented in Figure2 and Figure3

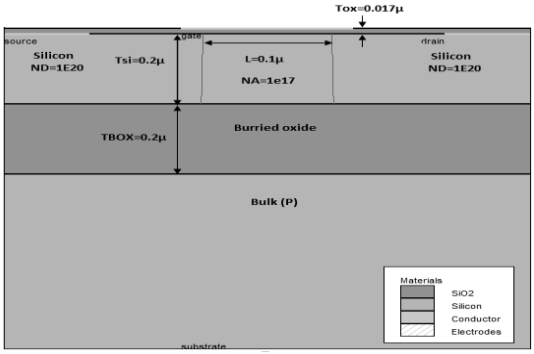

Figure 2. SOI n-MOSFET parameters.

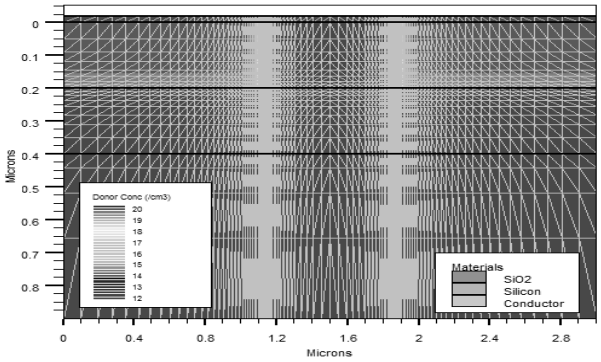

Figure 3. Device meshing

The different parameters of our SOI n channel enhanced transistor showninFigure 2are assumed as follows:

Drain and source length=1um, Gate length =1um, Channel length =1um, Gate oxide thickness t_{OX}=0.017um, Silicon film thickness t_{si}= 0.2µm, Buried oxide thickness t_{BOX}= 0.2um, Substrate doping =1x10^{17}cm^{-3}, Drain and source doping=1x10^{20}cm^{-3}. The structure shown in figures 2 is obtained for tsi= 0.2µm, that ensures a partially depleted channel. device meshing is shown in Figure3.

5.1. Influence of Silicon Body Thickness Variation on the Drain Current

Silicon film thickness is a key parameter, allowing designing a partially depleted or a fully depleted SOI MOSFET. In fact scaling silicon film thickness is desirable for better short channel behavior and reduced floating body effect. Consequently it is practical to consider the impact of silicon body thickness on the device performances. Figure 4(a) shows I_{DS}-V_{DS} characteristics for different silicon film thickness tsi.

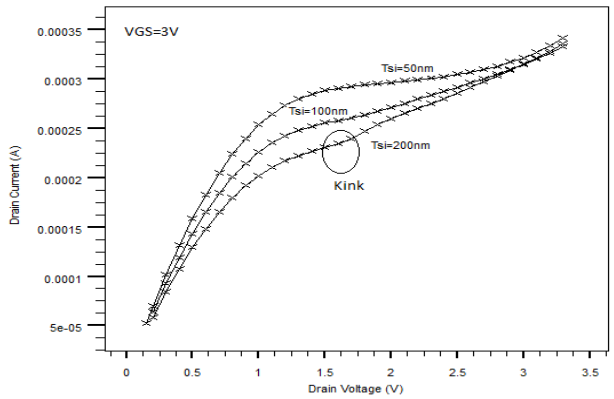

Figure 4(a). Output characteristics for different silicon film thickness tsi.

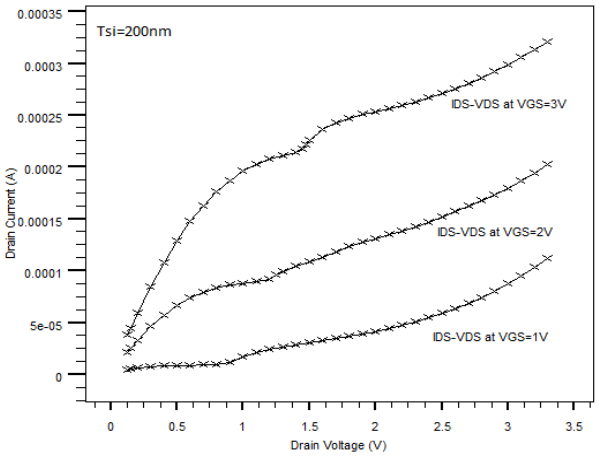

Figure 4(b) Output characteristics of the PDSOI n-MOSFET simulated.

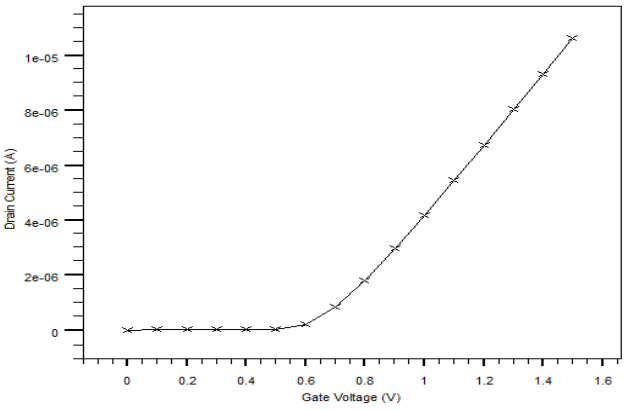

Figure 5. I_{DS}-V_{GS} characteristics of the PDSOI n-MOSFET simulated.

The output characteristics, shown in figure 4(b), exhibit a kink effect for a silicon body thickness equal to 0.2µ, essentially due to the floating body. In all the rest of our study, we maintain t_{si} value to 0.2µm. The I_{DS}-V_{DS} characteristics given in Figure 5 highlight a kink effect inherent in PD SOI transistors. The Presence of kink in these characteristics is clearly visible and belong to the so-called floating body effects. Depletion zone under the conducting channel does not extend sufficiently in-depth to reach buried oxide. Emergence of kink appears essentially for n-channel PD SOI MOSFETs above a certain value of V_{DS} voltage. At room temperature, Kink effect is not observed in bulk devices when substrate or well connections are provided, however kink effect can be observed in bulk MOSFET's operating at low temperatures. This effect is considered as the most important effects of the floating substrate, happening by the accumulation of carriers formed by impact ionization in the silicon film caused by high electric field near the drain region. In this case a part of the majority carriers which are

holes can migrate to the transistor body. This is principally due to the body potential V_B being firstly very close to V_S, that corresponds to zero. Whole migration leads to a local increase of V_B. If the voltage drop across the body-source diode is high enough, the junction may be switched, leading to a decrease of the transistor threshold voltage.We can also noticethat, in partially-depleted silicon thin-film SOI CMOS devices, due to the neutral region, an unsmooth transition in the drain current characteristics-kink effect is identified [15],[16].

5.2. Influence of temperature variation effects on the electrical characteristics of the device.

Knowing that SOI MOSFETs are conceived for applications where it is expected temperature variation or high temperature applications, we propose in this section to observe the impact of temperature variation on the electrical properties of our transistor.Typically, SOI MOSFET simulations are based upon the physical operation of the device, which exhibits both MOS and bipolar phenomena. As a result a more complex set of physical models will be required than for either MOS or bipolar technologies [14]. In order to study temperature variation effects, and based on
literature for SOI devices that have been intensively studies, , a set of typical models for a partially depleted SOI MOSFET have been used allowing taking into account the lattice heating (heat-flow). The numerical methods chosen for our simulations are Gummel and Newton methods.

5.2.1. Variation effects of the temperature on the PD-SOI n-MOSFET transfer characteristics

Figure 6, shows the simulated I_{DS}–V_{GS} characteristics for the simulated PD SOI n-MOSFET biased in the linear region (V_{DS} = 0.1V) and Figure 7 shows the same simulated characteristics in the saturation region (V_{DS}= 1.5V).

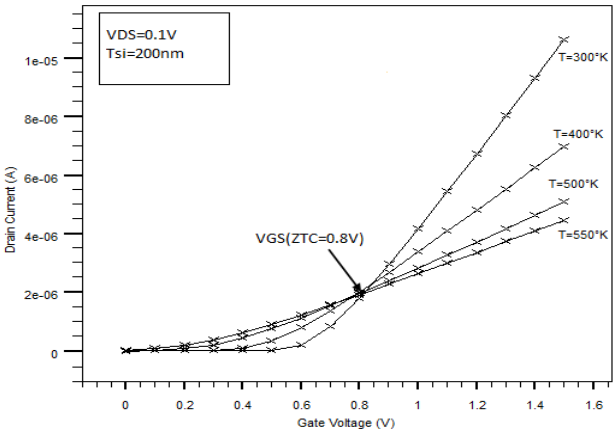

Figure 6. I_{DS}–V_{GS} transfer characteristics at differentoperating temperatures in linear region.

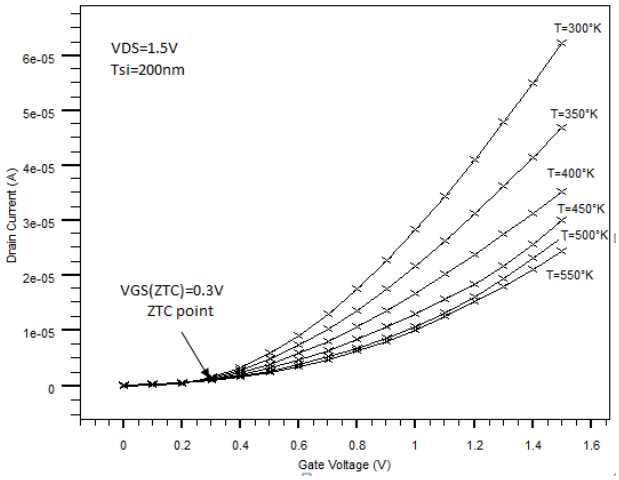

Figure 7. I_{DS}–V_{GS} transfer characteristics at different operating temperatures in the saturation region.

I_{DS}-V_{GS} plots allow extracting some electrical parameters of the structure such as the threshold voltage values. Our simulation results shown in Figures 6 and 7 highlight a particular V_{GS} voltage value for which the current is insensitive with the temperature fluctuation. In this significant operating point, the daring current is almost constant and independent of temperature variation. This common intercept point at different temperatures is called "ZTC point" a zero temperature coefficient bias [17]. Its existence can be explained by the fact that when the temperature increases, the threshold voltage decreases and V_{GS}-V_{TH}(T) term increases leading to I_{DS} increasing knowing that I_{DS} is proportional to V_{GS}-V_{TH}(T). At the same time, the mobility tends to decrease I_{DS} with temperature increasing for the reason that lattice scattering dominates at elevated temperatures leading to channel mobility diminution At low gate bias, V_{GS}-Vth(T) term dominates while at high gate bias, the mobility μ(t) term dominates.In summary we can say that the mobility tends to decrease I_{DS}, whereas the threshold voltage tends to increase this current. The consequence of this two temperature dependent parameters is the ZTC point. At this point the drain current is insensitive to temperature variation. Our simulation results allow us to note that V_{GS}(ZTC)=0.8V in linear region and V_{GS}(ZTC) =0.30V in saturated region. V_{GS}(ZTC) is lower in the saturation region. Biasing the transistor at V_{GS}(ZTC), leads to temperature independent behaviour. This property is use in some high performances applications. At theend of this section, we would like to recall a previous study developed by Shoucair, which helped to highlight the ZTC point of basic bulk MOSFETs .This ZTC point was up to 200°celsius [2].

5.2.2. Variation effects of the temperature on the PD-SOI n-MOSFET threshold voltage.

Threshold voltage variations with the operating temperature of our PD SOI n-MOSFET studied and extracted using ATLAS, are shown in Figure 8.

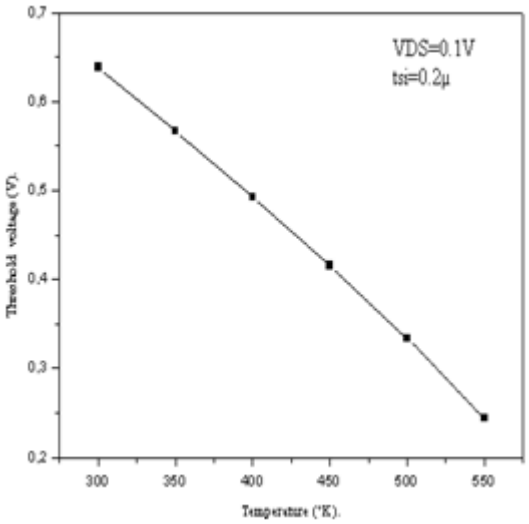

Figure 8. Variation of V_{TH} with operating temperature variation.

We can validate that V_{TH} decreases when the operating temperature decreases. In fact, threshold voltage temperature dependence comes from the energy bandgap, Fermi potential, and the depletion charge temperature dependence. The depletion charge temperature dependence is due to the Fermi potential dependence and Fermi potential temperature dependence is due to the temperature dependence of the intrinsic concentration ni, knowing that ni increases when the temperature increases while the Fermi potential and potential charge decrease lead to V_{TH} degradation [18].

5.2.3. Variation effects of temperature on the PD-SOI n-MOSFET transconductance "g_m" Characteristics.

Simulation results allowing observing temperature variation effects on g_m characteristics with the operating temperature of the partially-depleted SOI n-MOSFET device in a linear region are shown in Figures 9 and 10.

We can easily notice that the temperature has a direct impact on the gm-V_{GS} characteristics as shown in Figure 10. We can distinguish clearly, that for a weak inversion of the channel (V_{GS}< Vth,) the drain current is in fact attributable to diffusion and is known as subthreshold current .This leakage current increases with temperature increasing. Whereas for V_{GS}> V_{TH}, the channel is strongly inverted, this transconductance decreases with temperature increasing and this is mainly due to mobility degradation [19]. We can also observe, that a ZTC point can't be determined in linear region.

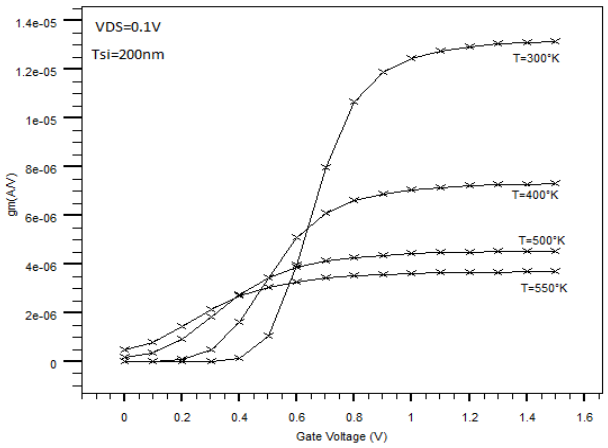

Figure 9. g_m-V_{GS} characteristics for the simulated PD SOI n-MOSFET at different operating temperature in the linear region.

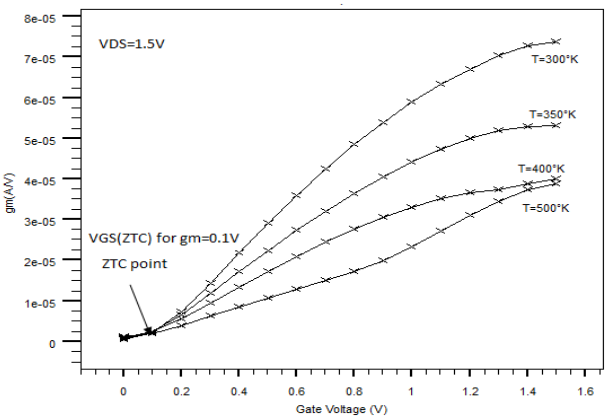

Figure 10. g_m-V_{GS} characteristics for the simulated PD SOI n-MOSFET at different operating temperature in the saturated region.

5.2.4. Temperature variation effects on the transistor output characteristics

Figure 11 exhibit the output plots for the simulated PD SOI n-MOSFET. These simulation results have shown the degradation of saturation current with rising temperature. At elevated temperature, the channel carriers mobility decreases due to lattice scattering leading to drain current reduction. It can also be noted that kink effect, principally due to holes generation accumulated in the neutral body as a result of impact ionization, is strongly reduced at high operating temperature as shown at T=400°K and 500°K.

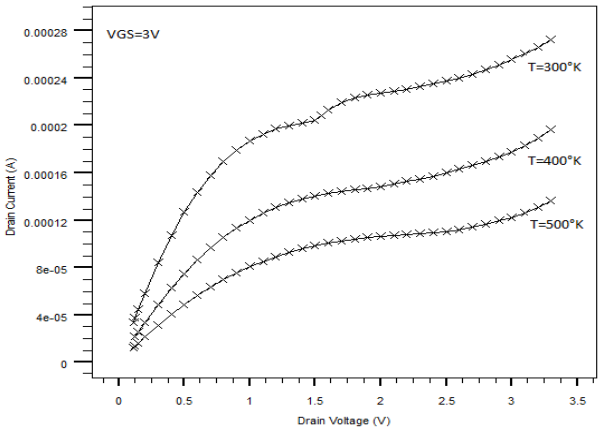

Figure.11. simulated output characteristics at different operating temperature.

5.2.5. Temperature variation effect on the transistor leakage current

A good comprehension of leakage current mechanisms in SOI CMOS technologies and leakage currents dependences on temperature is necessary in order to estimate the behavior of SOI CMOS technology for low-power circuits. The most important contributions to the off-state current in SOI MOSFETs are: the weak inversion current and the thermal generation current.

The cross section of SOI inverters and bulk CMOS inverters based on J.P.Colinge shown in Figure 12 and Figure 13 allow to illustrate the leakage components in SOI and Bulk technologies.

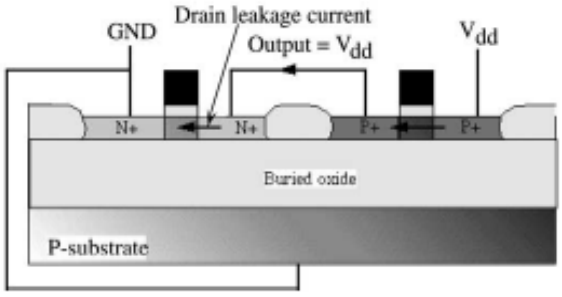

Figure 12. Cross-section of SOI inverters illustrating leakage components (based on Colinge) [11].

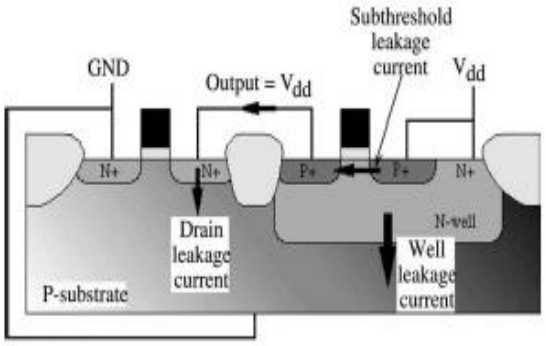

Figure 13. Cross-section of bulk CMOS inverters illustrating leakage components (based on Colinge) [11].

The OFF state current I_{OFF} is actually caused by thermal generation in the depletion region, in Bulk CMOS devices the most important source of thermal generation current shown in Figure 14 is the well junction that is more important than thermal generation at the drain junction, and this is mainly due to the large well area. In SOI devices, thermal generation current is reduced, and this lessening is due to the nonexistence of the well. As a general rule, the drain leakage current is 15–100 times smaller in SOI than in bulk MOSFETs [10]. However, in short-channel transistors, the weak inversion current becomes the most important contribution to off state leakage current in both bulk and SOI devices. This is essentially due to low V_{th}, necessary to maintain these short channel devices performances, and from Short channel effects leading to V_{TH} decreasing, and to subthreshold swing degradation that is smaller in SOI MOSFETS compared to bulk MOSFETS. Generally, a good device temperature behavioris needed and that because high performance SOI Integrated circuits are in fact conceived in order to operate at high temperature.However, it is found that off state

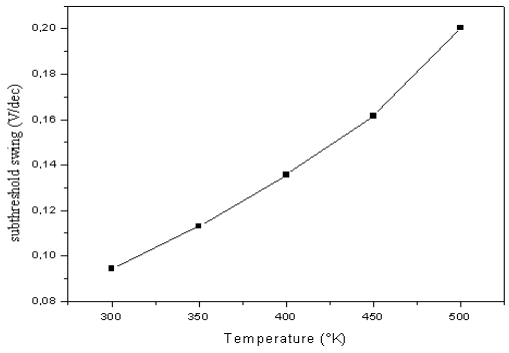

Figure 14. Subthreshold voltage variation with operating temperature variation.

leakage current increases when the temperature increases and this principally due to V_{TH} decreasing with operating

temperature increasing as shown in Figure 8. Subthreshold swing also increases with temperature increasing as shown in Figure 14 leading to the off state current increases.

Figure 15 and Figure 16 shown log I_{DS}-V_{GS} curves at operating temperature of 300,350,400, 450,500 and 550°K in both saturation and linear region. These simulations results we obtained allow investigating the temperature variation effects on the off state current of our device. As expected, the I_{off} leakage current increases with temperature increaing, both in linear and saturated region, and this was perfectly predictable.

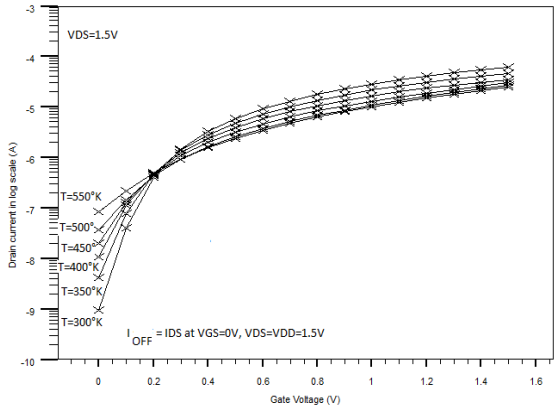

Figure 15. Temperature variation effects on the off state current for a partially depleted SOI n-MOSFET: in the saturation region (V_{DS}=1.5V).

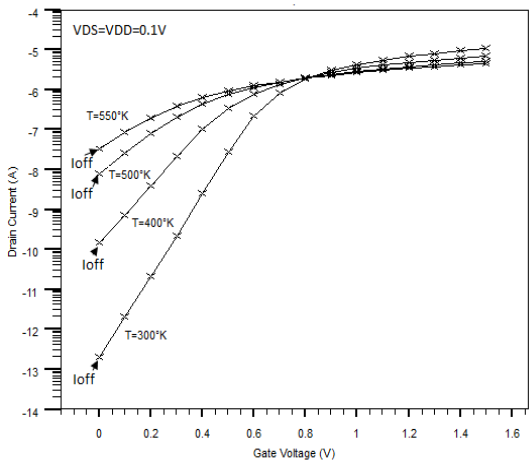

Figure 16. Temperature variation effects on the off state current for a partially depleted SOI n-MOSFET in linear region (V_{DS} =V_{DD}= 0.1V).

At the end of this section, we can affirm that the off state current increase with temperature is less significant in SOI CMOS technologies than in bulk CMOS and this is mainly due to: the lower dependence of the threshold voltage on the temperature for SOI devices, the better value of the subthreshold, the reduced short-channel effects, and the absence of well junctions for SOI devices [20].

5.3..Self heating effects

It is well known thatSOI devices exhibit self heating effects. Self heating effects arise because SOI devices are thermally insulated from the substrate by their buried oxide layer, leading to a significant elevation of temperature within the SOI device, which accordingly modifies the output characteristics of the device.

Self heating effects that have an important effect on drain current must be taken into accountt by device technology designers. In this work, tthermal and electrical effects are coupled through self-consistent calculations.

In Figure 17 the temperature distribution within our PDSOI n-MOSFETis shown. We can observe that the thin film's temperature appears to be upper than the external temperature that is room temperature T=300°K.

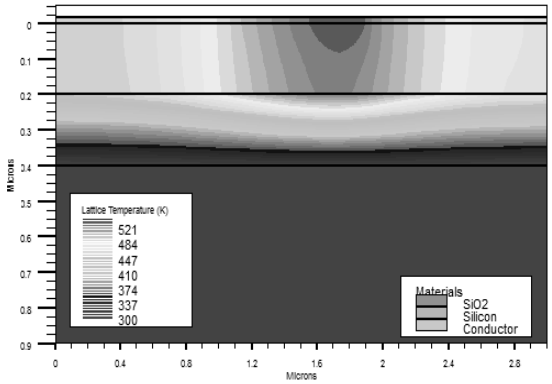

Figure 17: Temperature distribution within a partially depleted SOI n-MOSFET. External temperature is equal to 300 K.

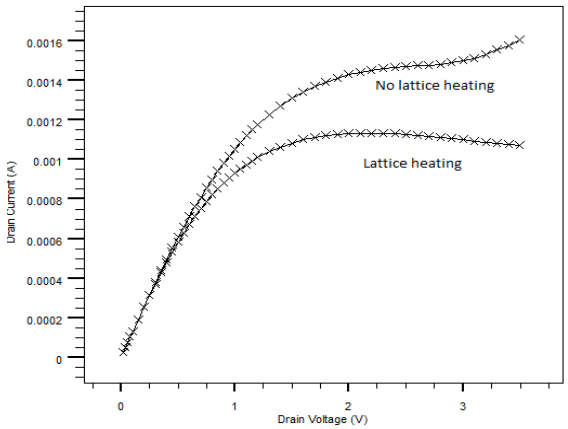

Figure 18. I_{DS}-V_{DS} with lattice heating and isothermal models.

Simulation results shown in Figure 18 allow comparing I_{DS}/V_{DS} curves for our SOI transistor using isothermal and non-isothermal approaches. We can observe that heating of silicon film causes a negative saturation slope.
that can be explain by the fact that at high temperatures, lattice scattering dominates and causes a carrier mobility reduction leading to drain current decreasing. Basically self-heating effects are more pronounced under higher drain and gate biases.

6. Conclusion

In this paper, all the device parameters considered in our investigations are fully simulated using SILVACO Atlas device simulator. The numerical simulation results, we obtained and relating to temperature variation effects on the electrical properties of partially depleted silicon on insulator n-channel MOSFET, are presented. Based on our results, we can conclude that the temperature has a significant impact on the device behavior. Our first conclusion was that kink effect in PD SOI n-MOSFET is strongly reduced at high operating temperaturedue to holes generation accumulated in the neutral body, as a result of impact ionization.Concerning the effects of temperature variation on the electrical characteristics of our device, we observed that the threshold voltage, the mobility and the drain current decreased when the operating temperature increased. This study also allowed us to highlight a bias point called ZTC point, where the drain current and transconductance show no temperature variations and to observe that ZTC point exists in both the linear and the saturation regions. In this study we have observe the temperature variation effects on the off state current of SOI MOSFETS. The I_{off} current of our device increases as the temperature increases, however, the off state current increase with temperatureremains very weak and is smaller in SOI CMOS technology than in bulk CMOS technology. At the end of this work self heating effects that affect the drain current in its saturation region, causing the Ageing of the device have also been presented.

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