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Performance study of a HEMT for power application

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Abstract

In this paper, we present a simulation results of the design and characterization for GaN double-gate transistor, that has T-gate geometries with high-electron-mobility to realize high performance using silvaco TCAD Software, this transistor is used for amplifiers application. We have obtained an excellent current density, almost 817mA/mm, a peak extrinsic transconductance of 915mS/mm at V_{DS}=2 V, and cutting frequency cutoffs of 878 GHz, and maximum frequency of 982 GHz.

Keywords— HEMT, GaN, power application, Tcad-Silvaco.

I. Introduction

Currently, Devices that work as a low-noise amplifier when the input signal level is low and automatically switches to high-power amplification for relatively high input signal levels [1] are the future of amplification.
For that we can enhance the performances of the next-generation with GaN-based high electron mobility transistors, we have created the structure using genetic algorithm and using Silvaco software tools for simulation.

The introduction of a thin AlN spacer layer at the InAlN/GaN interface, increases the carrier density and effectively reduces the alloy scattering of the two-dimensional electron gas (2DEG), so that it provides a better carrier confinement [2-3], InAlN/GaN heterostructure has good thermal stability and robustness, promising very high power and high temperature work operating mode [4].

A hydrodynamic or quantum model approach must be used to obtain accurate results for such structures. We propose quantum mobility models which corresponds to the particularities of the GaN material system. The models was implemented in our simulator Silvaco and carefully calibrated. A device from a recent transistor generation is simulated using the quantum genetic. A good accuracy for all relevant characteristics is achieved.
In this work, we have demonstrated that is possible to produce excellent properties of HEMT InAlN / GaN while minimizing side effects. Through the optimization of the device design and quality control of doping implant, also the adoption of several analytical models to simulate the devices highly scaled analysis characteristics [5], [6], in order to intentionally decrease phenomena unwanted until they become almost negligible.

2. Modeling Results

As illustrated in fig.1 (a), we see a cross section of the structure, and this structure located over the layer of substrate (4H-SiC). The device contact used an Au Schottky source/drain and gate electrodes, the device design features a heterostructure InAlN/GaN, where the periphery oxide Al_2O_3 of the Gate is a different than the conventional designs [7], and the passivation dielectric that minimizes surface leakage and creates a high density of shallow traps at the surface [8]. As a result, after a doping layer the leakage current density is eliminated from the device, resulting in an InAlN barrier undoped [9].

This raises the conduction band shape for the barrier that, for the same sheet carrier concentration based on Fujitsu model [10], The Hall mobility and sheet carrier concentration were 1300 $cm^2 V^{-1} s^{-1}$ and 1×10^{13} cm^{-2}.The heterojunction features a sheet charge density of $1.85x\ 10^{13}$ cm^2.Dimensions are also critical parameters for the device performance, the dimension of the device studied is given in Table 1.

Table 1 : Parameters of HEMT device.

Name	Symbol	Value [nm]
Thickness Cap Layer	E_{OH}	3
Thickness Layer Schottky	E_S	7
Thickness Layer Donor	E_D	3
Thickness Layer Spacer	E_E	1
Thickness Canal Layer	E_C	37
Thickness Tampon Layer	E_T	150
Thickness of Bulk	E_B	$100\ 10^3$
Length Drain Gate1	L_{DG}	$1.47\ 10^3$
Length Source Gate2	L_{SG}	$0.50\ 10^3$
Length Gate	L_G	15
Length Drain & Source	L_D	$0.5\ 10^3$

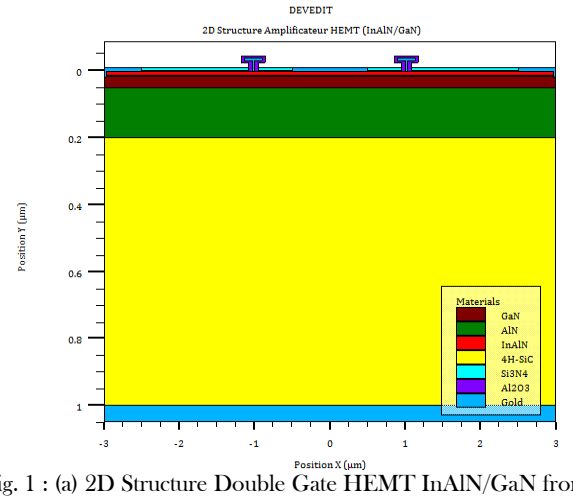

Fig. 1 : (a) 2D Structure Double Gate HEMT InAlN/GaN from Atlas.

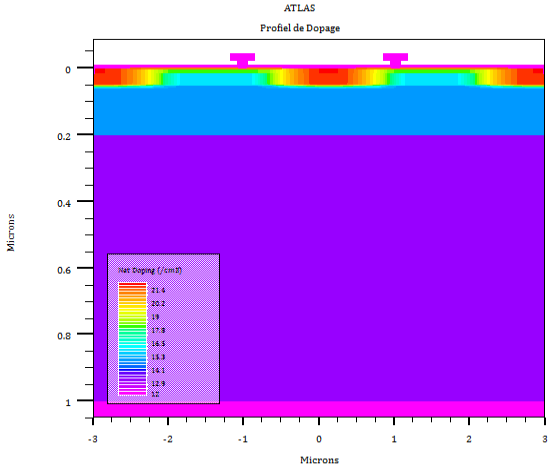

Fig. 2 : (b) Doping profile.

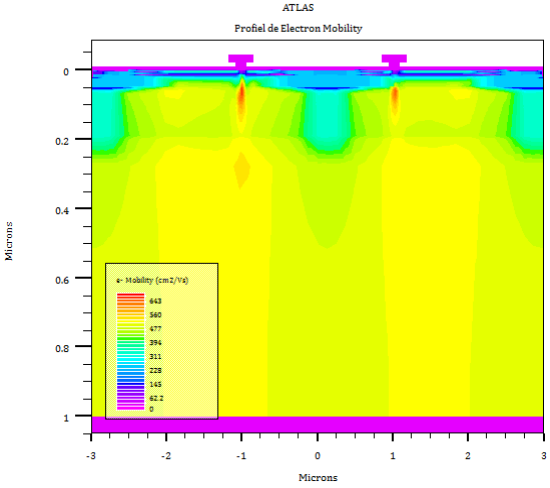

Fig. 3 : (c) Electron mobility.

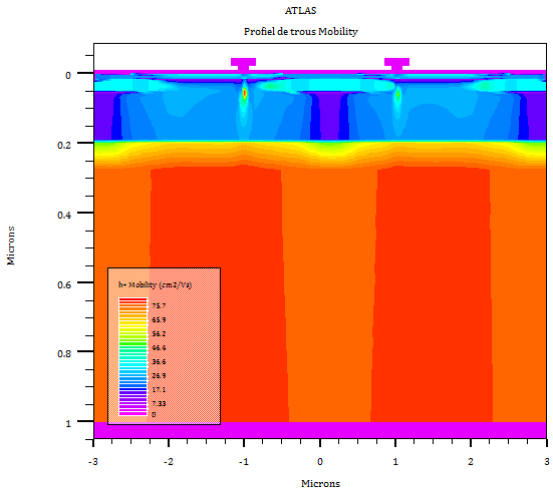

Fig. 4 : (d) Holes mobility.

3. Results and discussion

In this work, Silvaco ATLAS is used for the 2D simulation of the considered HEMT. Silvaco's ATLAS program performed the device structuring and subprogram calls, while BLAZE and GIGA, ATLAS sub-modules, perform special functions required for advanced materials, hetero-junctions, and thermal modeling. In fact, ATLAS generally uses the BLAZE program extension to correct model for the III-V semiconductors, in order to adapt calculations that involve energy bands at the hetero-structure. The hetero-junctions need to change in determination of current densities, recombination-generation and velocity saturation. The hydrodynamic with energy balance carrier transport model is used in order to achieve maximum accuracy as computational efficiency.

However, while using TCAD simulation software, some of physical models have to be incorporated into the model to perform desired simulations and do reliable predictions about our device characteristics.

These models deal with the carrier behavior such as lattice temperature. In addition, because of the high operating voltages, self-heating effects need to be considered in our simulations.

A. DC Results

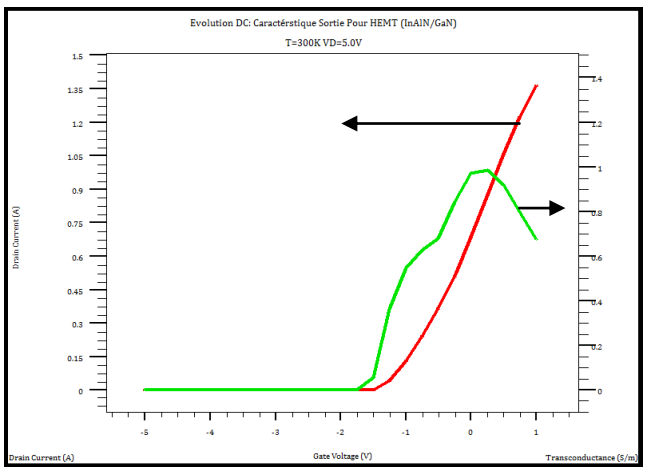

Fig. 5 : characteristics of HEMT InAlN/GaN with a gate length of 15 nm with V_{DS} 2.0 V.

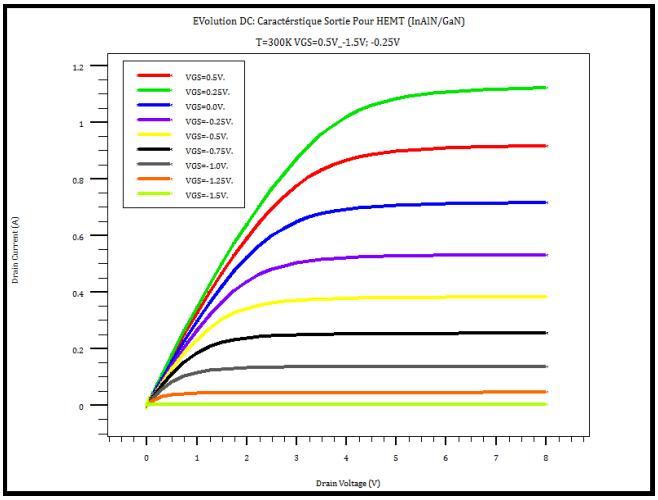

Fig. 6 : DC Output characteristics of DG-HEMT InAlN/GaN with a gate length of 15 nm with V_{GS} stepped from 0.25 V to −1.5 V in steps of −0.25 V.

In this simulation of the devices the electrical characteristics transfer is illustrated in right of the Fig. (2) The HEMTs with a gate length of the 15 nm, the device is delivered to extract an ON/OFF current density ratio higher than 1 x 10^{10}, and we have investigated the conduction band profiles to show that drain-induced barrier lowering (DIBL) is more explicit in a highly scaled device at length gate 15 nm,DIBL=33.52mV/V with V_{DS} fixed between 2 V and V_{DD}, effects due to this length of the gate which are observed are called short-channel effects (SCE). Effects occurring at larger V_{DS} are termed drain induced barrier lowering (DIBL) effects [11]. We are not the first to observe this in simulations for HEMTs, it has been investigated since 1989 by Awano and al. [12].

Fig. (2) in left we have presented the extrinsic transconductance characteristics of the device at V_{DS}=2 V, the simulated exhibits a maximum as 915mS/nm at V_{GS}=0.0 V. This peak shows in the curve of the transconductance a dependence on gate bias V_{GS} and obviously reflects the DC behavior of the simulated HEMT, which correspond to the 2DEG channels modulated by different gate voltages. These properties are superior to the values previously reported for similar structures based on AlGaN/GaN heterostructures [13]. Here, a better DC characteristic is realized on sample with slight inferior electrical properties in comparison with the earlier reported [14], the total parasitic resistance generally is dominated at low Ohmic contact resistance for this is to highly desirable, which could be attributed to the increased carrier concentration or/and an increased carrier mobility [15].

We have changed the drain voltage between 0V and 3V, when simulation is first conducted to obtain the I-V characteristic in DC mode to change the state of the gate voltage by 10 different bias, V_{GS} = 0.25 V to - 1.5V with the step of the -0.25V for both HEMTs. The positive increase in the drain voltage, leads to the electric field across the channel increases the speed of the electron. The voltage distribution across the channel leads to a voltage difference between the gate and the channel along it, the transistor taking a variable resistance behavior controlled by the gate voltage. Indicating excellent gate control of the 2DEG channel [16], and the maximum drain current available reached 817 mA/mm when V_{GS} was biased at 0.0 V & V_{DS}=3.0V. The pinchoff voltage is extracted at −1.5 V. show in Fig. 3.

B. AC Results

We Show in this simulation the gain of the current H_{21}, unilateral (U_T), max transducer (MGT), maximum stable (GMS) and maximum available (GMA) for power gain versus frequency range of [1 GHz to 1 THz] in fig 5.

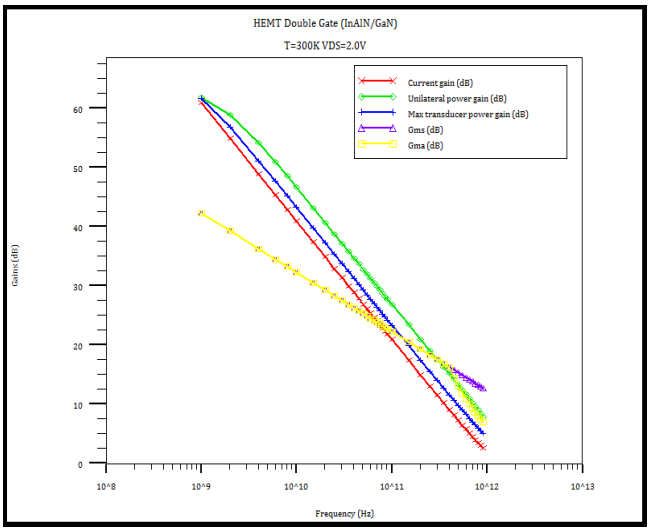

Fig. 7 : Simulated current gain (H_{21}), Unilateral (UT), max transducer (MTG), max available (GMA) and Max stable power gain (GMS) versus frequency for the L_G=15nm InAlN/GaNHEMTs. The bias were V_{DS}=5VandV$_{GS}$=0V.

This result values extracted after verifying from the extrinsic S-parameters with the intrinsic values of this device by simulation with extrinsic parameter models, due to the effect of the capacitances of the high gate to source capacitance (C_{GS}) resulting from the extended effective gate length [18], and the electronic transfer in the channel is optimized.

The cutoff frequency is 978 GHz and the value of Max frequency is approximately of 889 GHz with a slope of 0 dB/Dec for the device, this value is greater than DG-HEMT and may be used for future low noise MMIC design applications.

Inset shows that the peak value of GMS and GMA is obtained as 42 dB and for U_T, GMT and H_{21} are 61 dB, 62 dB and 63 dB through simulation respectively. A steep decrease is observed up to around 0 dB for frequencies even it is greater than 1 THz. This indicates good stability performance exhibited by the device making it suitable for low-noise amplifier applications.

The rise in the value of the frequency of the pieces show the basis for being associated with the length of the gate, gas electron two-dimensional gas is double 2DEG in the canal, as well as the design of the device. For comparison, the highest ft reported so far in nitride transistors double gate was the device is enhanced and very impressive f_T and f_{Max} peak values of 668 GHz and 312 GHz are obtained respectively [19].

4. Conclusion

In this paper, we have reported high-efficiency GaN HEMT on SiC substrates using the periphery Al2O3 oxide periphery of the gate and the mince InAlN barrier for

amplifier applications. Balanced device was designed and simulated by using a GaN HEMT by Tcad-Silvaco software.

The results prove that the proposed GaN HEMT amplifier can deliver the highest power and higher efficiency performances for power applications.

References

[1] Kevin W. Kobayashi, Torrance, C A, "Hemt-hbtdoherty microwave amplifier", BREVET, CA2389477 A1, 2002.

[2] R. Tulek and al. "Comparison of transport properties of high quality AlGaN/AlN /GaN and AlInN/AlN/GaN heterostructures with two-dimensional electron gas", J. Appl. Phys 2009, 105 :0137071- 0137072.

[3] A. Teke, S. Gökden, R. Tülek, J.H. Leach, Q. Fan, J. Xie, Ü. Özgür, H. Morkoç, S.B. Lisesivdin, E. Özbay, "The effect of AlN interlayer thicknesses on scattering processes in lattice-matched AlInN/GaN two-dimensional electron gas heterostructures", New J. Phys. 11, pp. 1-2, 2009.

[4] E. Kohn, F. Medjdoub,"InAlN – A new barrier material for GaN-based HEMTs", in: International Workshop on Physics of Semiconductor Devices 2007: 311 – 316, Mumbai, India.

[5] M. Uren, K. Nash, R. Balmer, T.Martin, E.Morvan, N. Caillas, S. Delage, D. Ducatteau, B. Grimbert, and J. De Jaeger, "Punch-through in shortchannelAlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 2, pp. 395–398, Feb. (2006).

[6] S. Kumar, A. Agrawal, R. Chaujar, S. Kabra, M. Gupta, and R. Gupta, "Threshold voltage model for small geometry AlGaN/GaN HEMTs based on analytical solution of 3-D Poisson's equation," *Microelectron. J.*, vol. 38, no. 10/11, pp. 1013–1020, Oct./Nov. (2007).

[7] http://www.silvaco.com/examples/tcad/section31/example3/index.html, "25-nm n-MOSFFET with quantum correction"

[8] Massachusetts Institute of Technology (MIT) and IQE "RF LLC have used an aluminum gallium nitride (AlGaN) back-barrier to improve the frequency performance of indium aluminum nitride (InAlN) high-electron-mobility transistors (HEMTs)"[Dong Setup Lee et al, IEEE Electron Device Letters, Mar (2011), USA.

[9] N. Ramanan, B. Lee and V. Misra, "Device Modeling for Understanding AlGaN/GaN HEMT Gate-Lag", IEEE Transactions On Electron Devices, Vol. 61, No. 6, pp 2012-2018, (2014).

[10] D.-H. Kim et al, "30-nm InAsPseudomorphic HEMTs on an InP Substrate With a Current-Gain Cutoff Frequency of 628 GHz", IEEE Electron Device Letters, vol. 29, no 08, p. 830-833, (2008).

[11] G. Krokidis , J.P. Xanthakis , N.K. Uzunoglu, "A fully 2-dimensional, quantum mechanical calculation of short-channel and drain induced barrier lowering effects in HEMTs", Solid-State Electronics 52, pp.625–631, 2008.

[12] Y. Awano, M. Kosugi, K. Kosemura, T. Mimura, M. Abe, "Short channel effects in sub quarter-micrometer-gate HEMTs: simulation and experiment", IEEE Trans Electron Dev;36 (10), 2260–6, 1989.

[13] Z. Tang, S. Huang, Q. Jiang, S; Liu, C Liu and K. J. Chen, "600 V High-Performance AlGaN/GaN HEMTs with AlN/SiNx Passivation", CS MANTECH Conference, May 13th - 16th, 2013, New Orleans, Louisiana, USA.

[14] R. M. Chu, Y. G. Zhou, J. Liu, D. Wang, K. J. Chen, and K. M. Lau, "AlGaN-GaN double-channel HEMTs", IEEE Trans. Electron Devices 52, pp. 438, 2005.

[15] J. S. Xue, J. C. Zhang, Y. W. Hou, H. Zhou, J. F. Zhang, and Y. Hao, "Fabrication and characterization of InAlN/GaN-based double-channel high electron mobility transistors for electronic applications", J. Appl. Phys. 111, pp. 114513 , 2012.

[16] B. Tian, C. Chen, J. Zhang, et al., "Structure and electrical characteristics of AlGaN/GaN MISHFET with Al_2O_3 thin film as both surface passivation and gate dielectric". SemicondSciTechnol, 2011, 26: 085023.

[17] W. Chung, E. Hoke, M. Chumbes, and T. Palacios,"AlGaN/GaN HEMT With 300-GHz fmax", IEEE Electron Device Letters, Vol. 31, No. 3, pp.197, Mar 2010.

[18] H. Pardeshi, G. Raj, S. Pati, N. Mohankumar& C. K. Sarka, "Influence of barrier thickness on AlInN/GaN underlap DG MOSFET device performance", Superlattices and Microstructures V. 60, pp. 47–59.

[19] T. lee, "Terahertz electronics: Opportunities, challenges and technologies", International Symposium VLSI Design, Automation, and Test (VLSI-DAT), pp. 1, 2013.