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Modeling and Design of Integrated Solenoid Inductor for SRF

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Abstract. As the demand for portable electronic devices increase, the need to replace off-chip discrete devices with on-chip devices is imperative. Inductors are one such passive device that is widely used in low noise amplifiers, oscillators, etc. Current on-chip spiral inductors suffer from large parasitic and area for a meager value of inductance and quality factor. In this paper, we discuss the design of integrated solenoid Inductor for Silicon Radio Frequency (SRF). The changes in the value of the inductance, resistance, quality factor and parasitic are studied for varying number of turns of the coil and spacing between turns. An optimum design incorporating the least parasitic and reasonable inductance is proposed.

Keywords: *Integrated inductor, Silicon Radio Frequency (SRF), On-chip spiral inductor*

1. Introduction

An ideal inductor can be defined as one that has a pure inductance, with no resistance or capacitance terms. In simple terms an ideal inductor is one that does not dissipate or radiate energy. However, a real inductor's performance is determined by its layout design and its physical characteristics regarding the loss mechanisms like resistive losses of the metal windings and substrate losses [1]. Thus, the inductance value obtained from simulating the above structure in Figure 1 does not represent the absolute value of the inductance of the coil. The main hindrance is the presence of parasitic [2] comprising of stray capacitances and resistances like:

- Coupling capacitance between the turns of the coil in both metal-1 and metal-2
- Capacitance of the oxide (Cox)
- Capacitance of the silicon substrate (Csub)
- Eddy current effects due to the resistance of substrate (Rsub)
- Resistances of the metal-1 and metal-2 and via-1 (Rs)
- Fringing capacitance of the coil (Cf)

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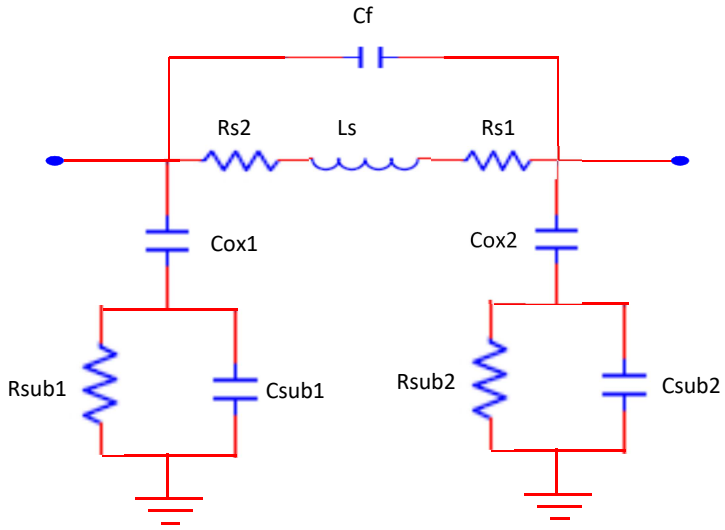


Fig. 1: Model electric of inductor

At high frequencies, the stray capacitances begin to affect the inductor's behavior, and at a certain frequency, real inductors can behave as resonant circuits, becoming self-resonant. At frequencies above this, the capacitive reactance becomes the dominant part of the impedance and the inductor has no significance. At higher frequencies, resistance and resistive losses in inductors increase significantly due to skin effect in the inductor's winding wires. Core losses also contribute to inductor losses at higher frequencies. Given the three-dimensional structure of the inductor, there can be other unforeseen losses in the coil and substrate.

2. Inductor design

The schematic of an inductor with magnetic core listing various parameters used in the representative model [3] model are shown in Figure 2. *N* is the number of turns of the coil, *Lc* is the length of the coil, *La* (*Lm*) is the length of the air core (magnetic core), *Wm* is the width of the magnetic core, *Wv* is the width of the via, *Gv* is the via overhang, *Sv* is the via size, *Sp* is the spacing between turns, *Wa* is the width of the air core, *Tc* is the thickness of the coil, *Tm* is the thickness of the magnetic core, *Ta* is the thickness of the air core and *H* is the height of the structure [4].

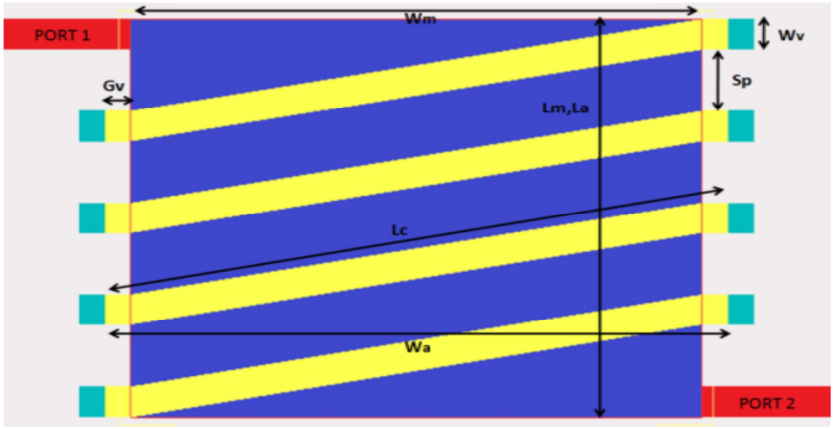
The expression for the inductance of the integrated solenoid inductor with air core, L_{AC}, is modified from the Wheeler formula based on the comparison with the experimental and simulation results [5] and can be written as:

$$L_{AC} = L_{Winding} + L_{Parasitic} \tag{1}$$

Where:

$$L_{Winding} = \frac{10\pi\mu_0 a^2 N^2}{9a + 10L_a} \tag{2}$$

$$a = \sqrt{\frac{(W_a + 2S_v)(T_a + 2T_c)}{\pi}} \tag{3}$$



(a)

(b)

Fig. 2: Integrated solenoid inductor with magnetic core: a) top view and b) cross-sectional view.

The winding inductance $L_{Winding}$ depends on the cross section area of the core, which includes the vias and the coils surrounding the air core. The parasitic inductance $L_{Parasitic}$ represents effects due to parasitics at the ports. Upon the introduction of a magnetic core, the inductance should be enhanced by the relative permeability (μ_r) of the core [6].

$$L_{Solenoid} = \frac{\mu_0 \mu_r N^2 W_m T_m}{L_m} \tag{4}$$

At lower frequencies, the expression for series resistance [7] is expressed as a sum of the resistances of the coil over the air core, the connection to the via and the via itself.

$$R_{AC} = 2N\rho\left[\frac{T_c}{W_m T_c} + \frac{(S_v + 2G_v)}{W_v T_c} + \frac{T_c + T_a}{S_v^2}\right] \tag{5}$$

Where, ρ is the electrical resistivity of the coil material. At higher frequencies the current tends to flow on the surface of the conductor making the effective current carrying cross sectional area smaller than that at lower frequencies [8].

Another important parameter that decides the usefulness of an inductor is the quality factor (Q). It is defined as the ratio of the energy stored to the energy dissipated in the circuit. The energy is stored in the inductive and capacitive elements in terms of magnetic and electric field and the energy is dissipated by the resistances in the circuit in the form of heat. The quality factor [9, 10] is frequency dependent and can be written as:

$$Q = \frac{\omega * Maximum.energy.stored}{Power.Loss} \tag{6}$$

$$Q = \frac{\omega}{\Delta\omega} = \frac{f_r}{\Delta f} \tag{7}$$

Where $\omega = 2\pi f_r$ is the angular frequency and f_r is the resonant frequency and Δf is the bandwidth of the circuit. The equations (1) through (7) provide a rough estimate to the values of inductance, series resistance and quality factor. The practical values as we see in the simulation results ahead vary quite a bit from the theoretical values.

3. Results and discussion

Figure 3 shows the inductance of the coil with increase in spacing. All three numbers of turns follow the same behavior for a given structure but have different peak inductance values. The maximum inductance is 138 nH at 3 GHz. The parasitic capacitances such as the oxide capacitance, coupling capacitance between turns and turns to core, and the fringing capacitance all resonate with the series inductance forming a parallel resonant circuit. The effect of capacitance between the turns, and from turns to core is maximized with increasing number of turns for a given area. It is observed that for the given configuration, the inductance tends to reduce with increase in spacing.

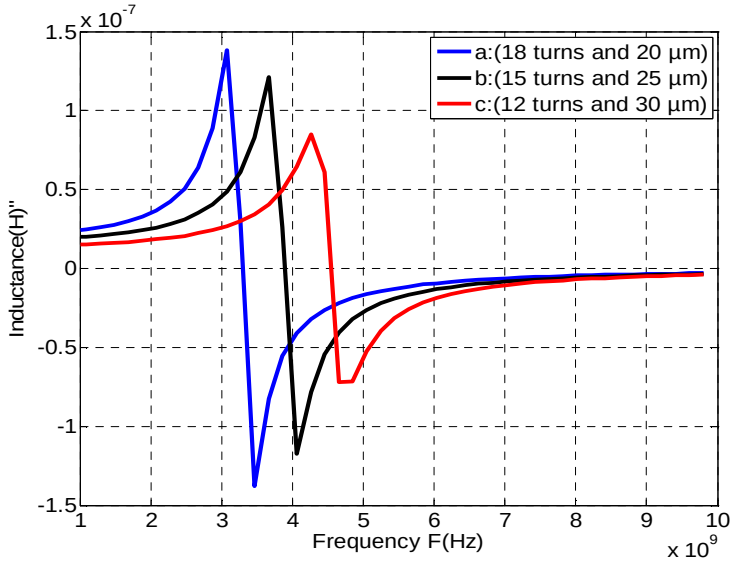


Fig. 3: The inductance for a spacing of: a) 18 turns and 20 µm, b) 15 turns and 25 µm, c) 12 turns and 30 µm

Figure 4 shows the quality factor of the inductor. The quality factor becomes zero at the resonant frequency because the inductance/capacitance values are also zero at the same frequency, implying that there is no energy stored in the circuit. The quality factor for (b) is 10 at 2.2 GHz, which is higher than the peak of 8.3 at 2.1 GHz for (a). This increase in quality factor can be attributed to the lowering of resistance, and hence, a drop in the power consumed by a smaller coil length. (c) Shows a lower peak compared to (b) and this may be due to the fact that the increased spacing now affects the inductance to a greater extent such that the drop in inductance value causes a drop in the quality factor. The damping nature of values with increasing frequency observed in all the graphs are due to the skin effect, parasitic and other core losses. Therefore a tradeoff can be made between number of turns and spacing depending on the parameter of interest.

Figure 5 show a peak of 241 Ω at 2.6 GHz, 198 Ω at 3.8 GHz and 175 Ω at 5 GHz. The drop in resistance for 30 µm spacing is the maximum compared to 30 µm spacing of turns. The structure used for (18 turns and 20 µm) has the highest number of turns compared to the rest and hence a large coil length. This increases the resistance of the coil as well as the parasitic. With the increase in spacing and reduced number of turns, the resistance can be decreased by a large amount.

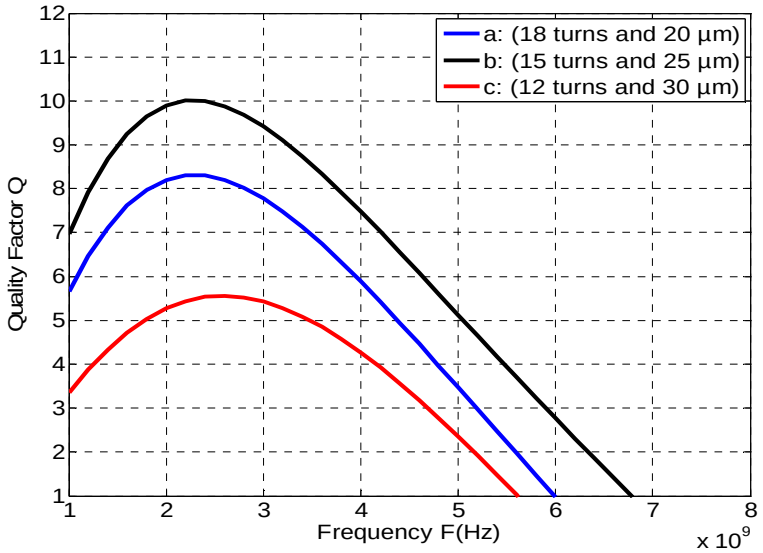


Fig. 4: The quality factor for a spacing of: a) 18 turns and 20 µm, b) 15 turns and 25 µm, c) 12 turns and 30 µm

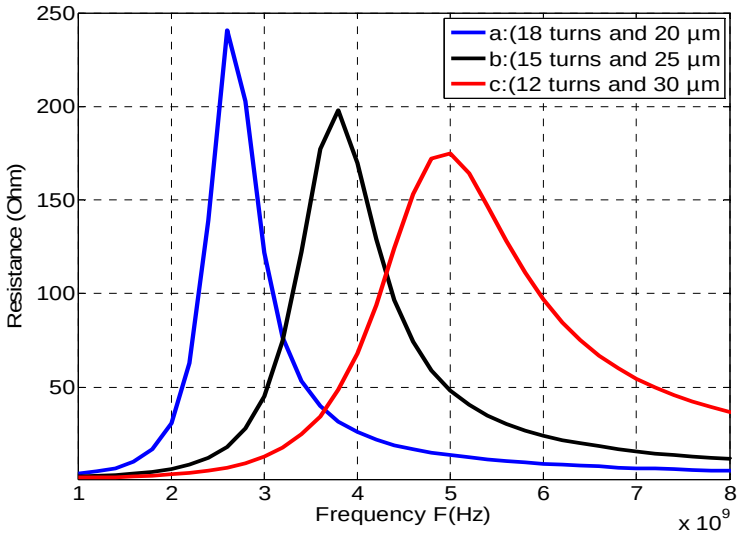


Fig. 5: The resistance for a spacing of: a) 18 turns and 20 µm, b) 15 turns and 25 µm, c) 12 turns and 30 µm.

4. Conclusion

Increasing the spacing between turns helped increase the quality factor but reduced the inductance upon very large spacing. A spacing of 40 µm showed the highest *Q* for the given structure. Large spacing implies lower number of turns for a given area meaning lower inductance. Hence, there is a tradeoff between number of turns and spacing. The parasitic capacitances form a parallel resonant circuit with the inductor and cause resonance in the circuit, creating damped oscillations. These oscillations disappear with the increase in spacing between turns.

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